FEC Firmware Upgrade Tutorial

1 FEC programming using the Xilinx Impact software

1.1 Installing the Xilinx Impact software

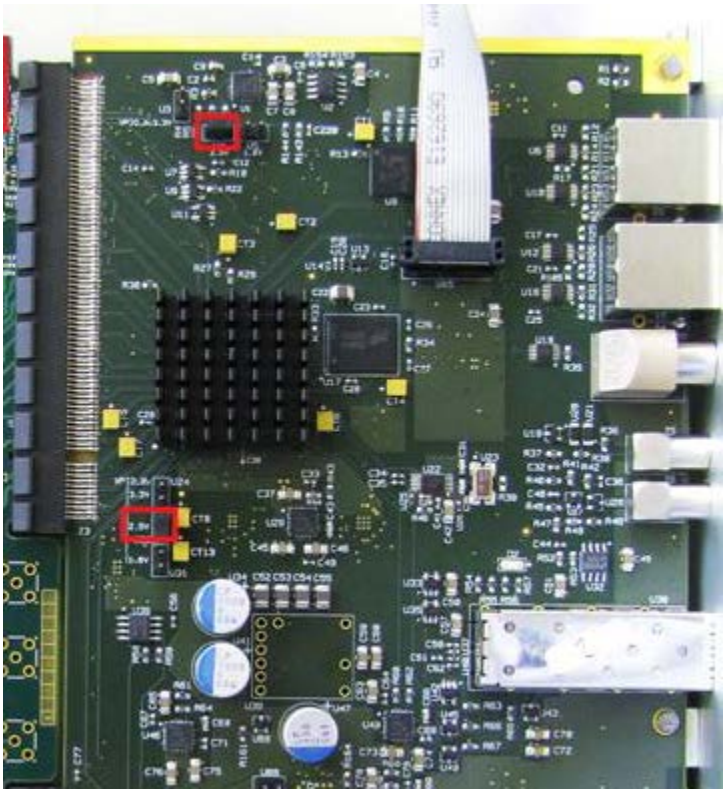
Go to the Xilinx.com website section Products -> Design Tools and download and install the free ISE WebPACK. If you have access to a full installation package (eg. CERN dfs) you can install the "Lab Tools" only, which will install Impact without the need to purchase or request a licence. The Xilinx software supports both Linux and Windows platforms.

You will also need to use the Xilinx Programmer cable (Platform Cable USB II)

You can find more information about alternative programming options from the Xilinx website, in the Products – Technology - Configuration Solutions section. In particular Digilent offers programming solutions compatible with the Xilinx software (for more details go to http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,395&Cat=5)

1.2 Connecting the Xilinx programming dongle to the FEC card

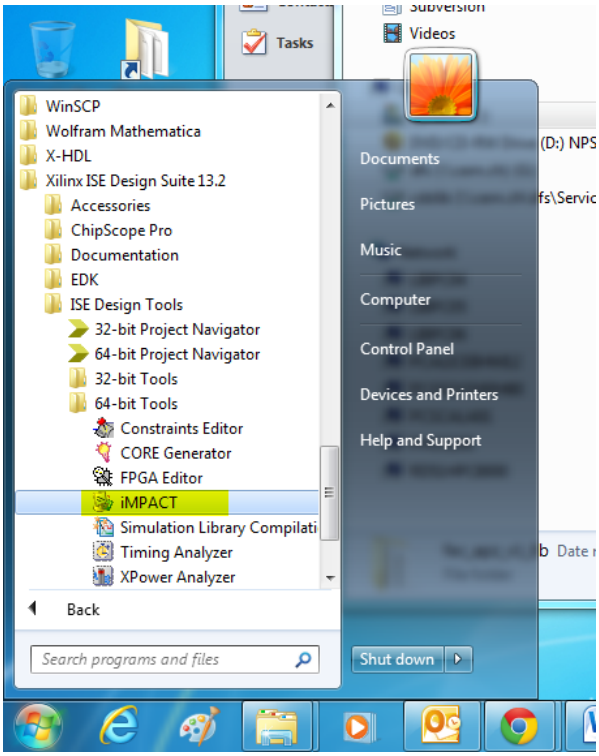
a) Connect the Xilinx Programmer to the PC and wait until it is recognized and the corresponding drivers are automatically installed (Windows)
b) Make sure the FEC card is switched off, then connect the flat cable of the Xilinx Programmer to the corresponding FEC connector (U15)



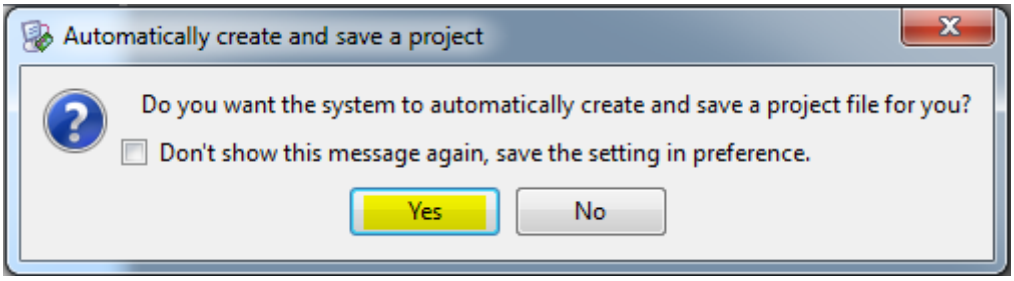
c) Power on the FEC card. If power conditions are ok, the light on the Xilinx Programmer will turn green.

1.3 Programming the FEC board

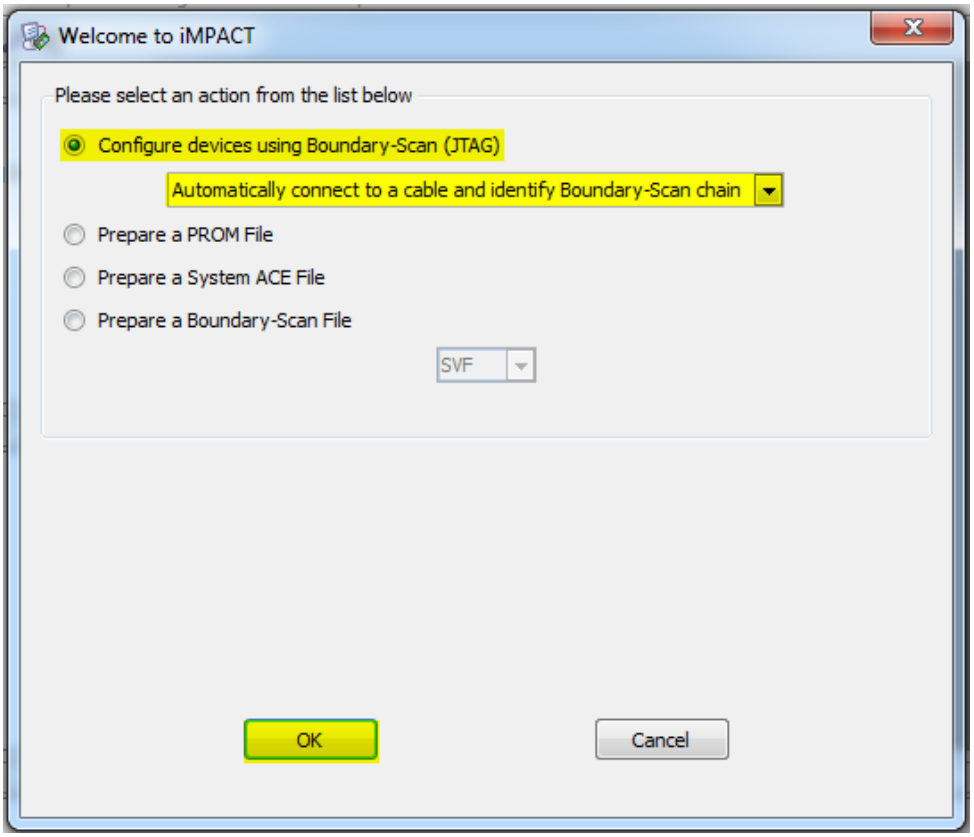
a) Start the Impact software from the Start Menu:



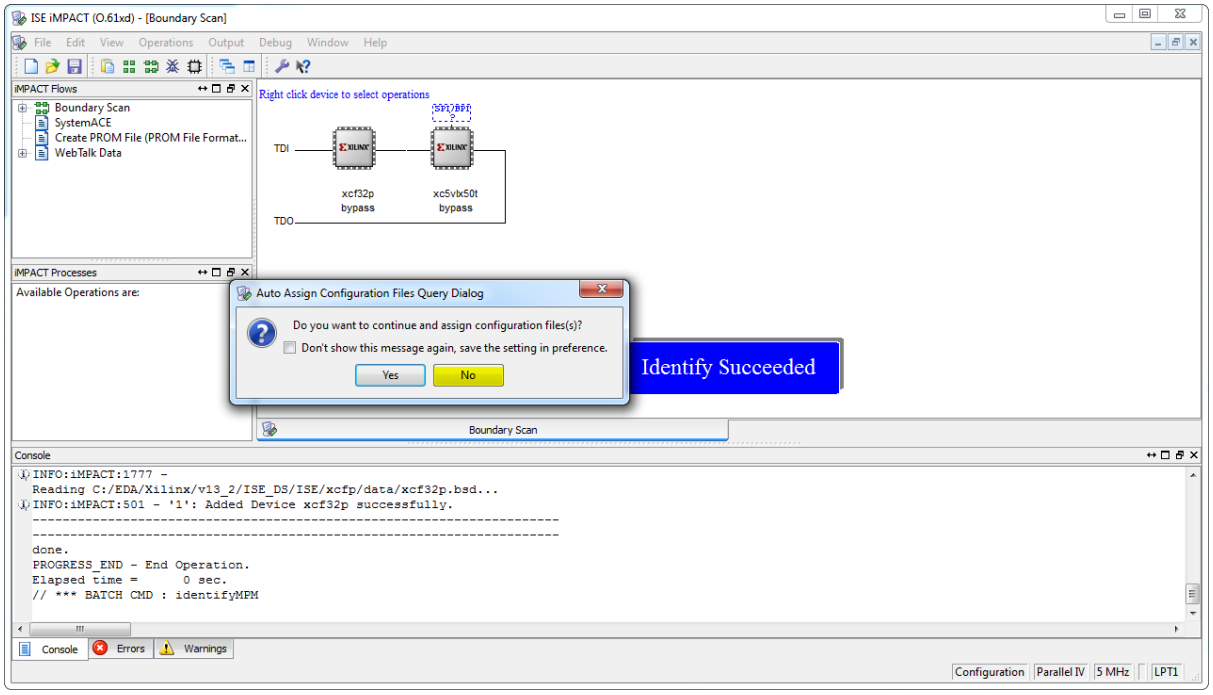
b) Answer *Yes* when asked to create a project



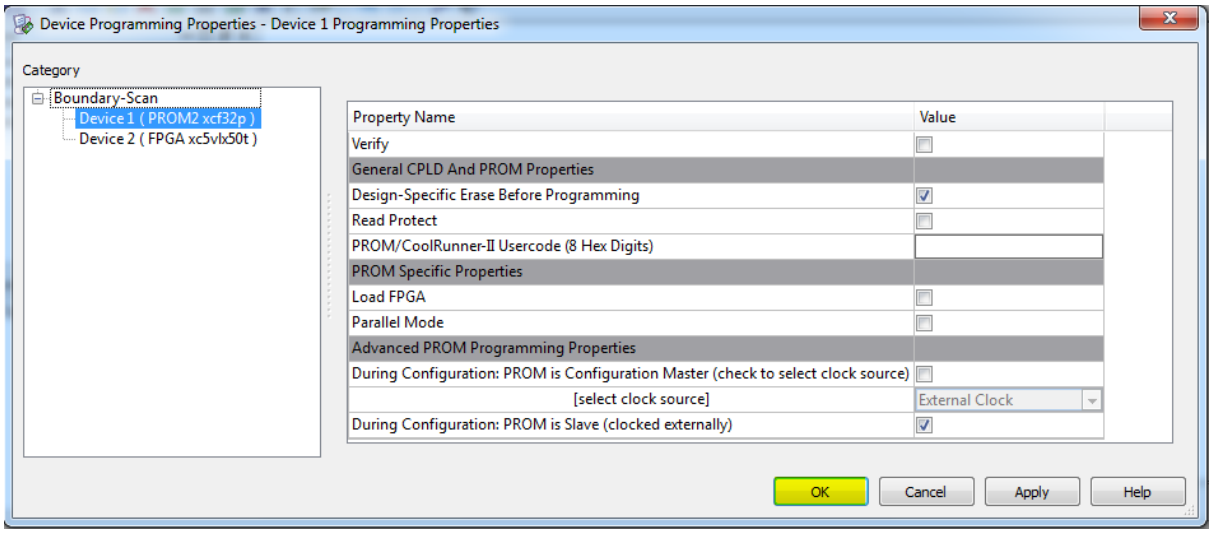
c) Make sure that *…Boundary-Scan (JTAG)* is selected and press OK



d) The program will automatically identify the devices EEPROM and FPGA devices present on the FEC JTAG chain. Press *No* when asked to automatically assign configuration files.



e) Press *OK* to accept the default programming parameters

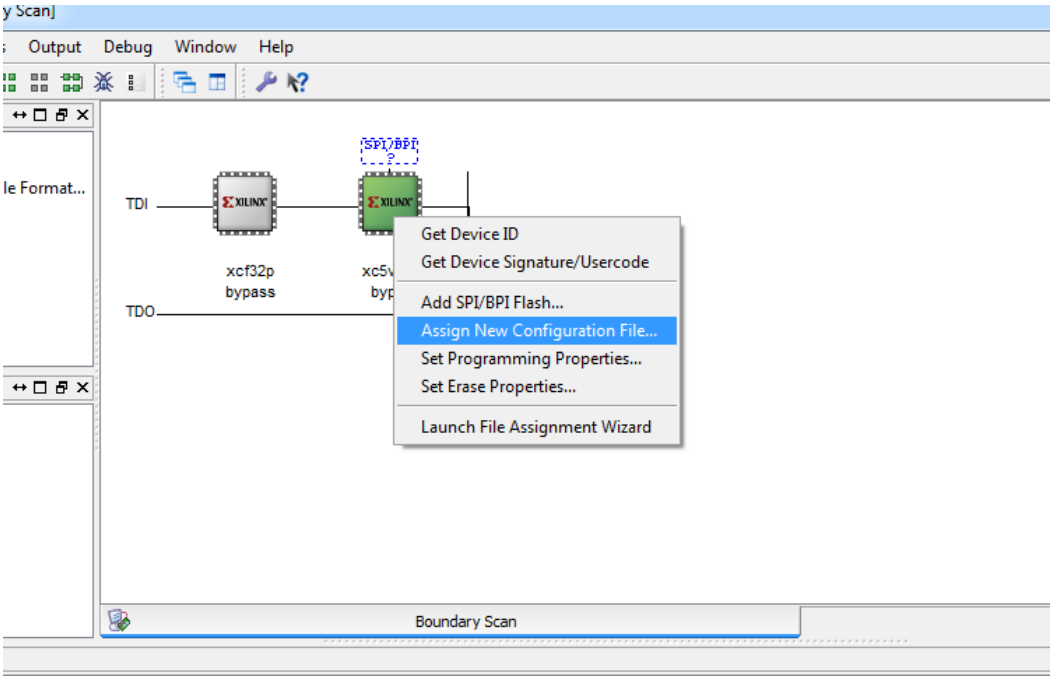


1.3.1 Temporarily programming the FEC FPGA

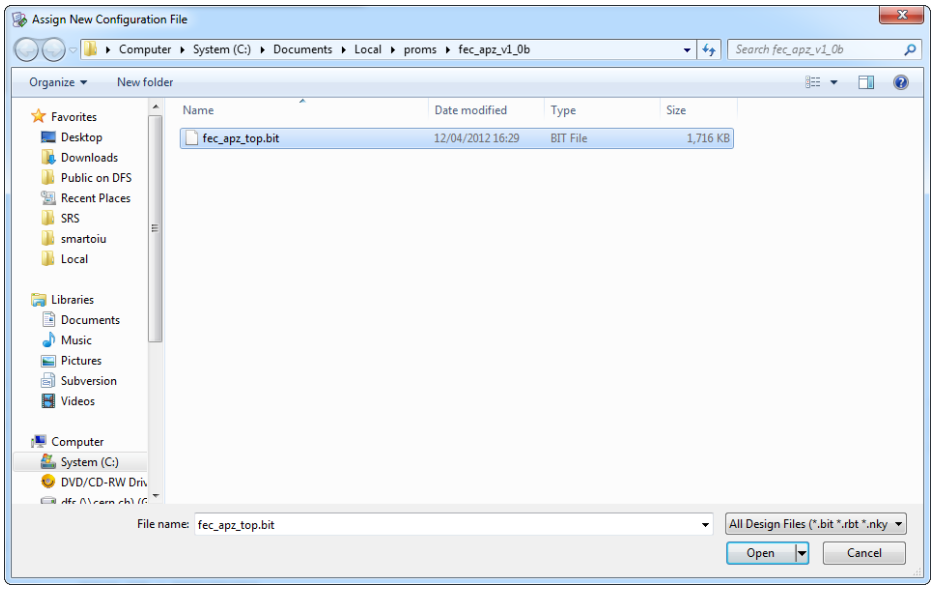
The firmware can be loaded directly into the FPGA without writing it permanently to the on-board EEPROM. This operation is useful for testing a new firmware update with minimum risk. At the next power cycle, the FPGA will boot with the default firmware stored on the local EEPROM. If you want to continue testing the new firmware you need to reload it to the FPGA.

If you want to permanently write the new firmware to the FEC board, go to next section (1.3.2 Program the on-borard boot EEPROM (permanent programming))

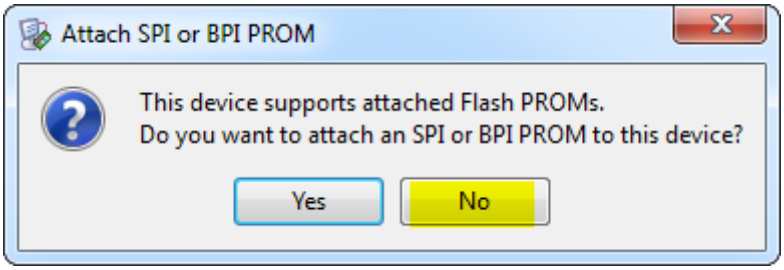
a) On the Boundary Scan tab right-click on the FPGA device (xc5vlx50t) and select *Assign New Configuration File …*



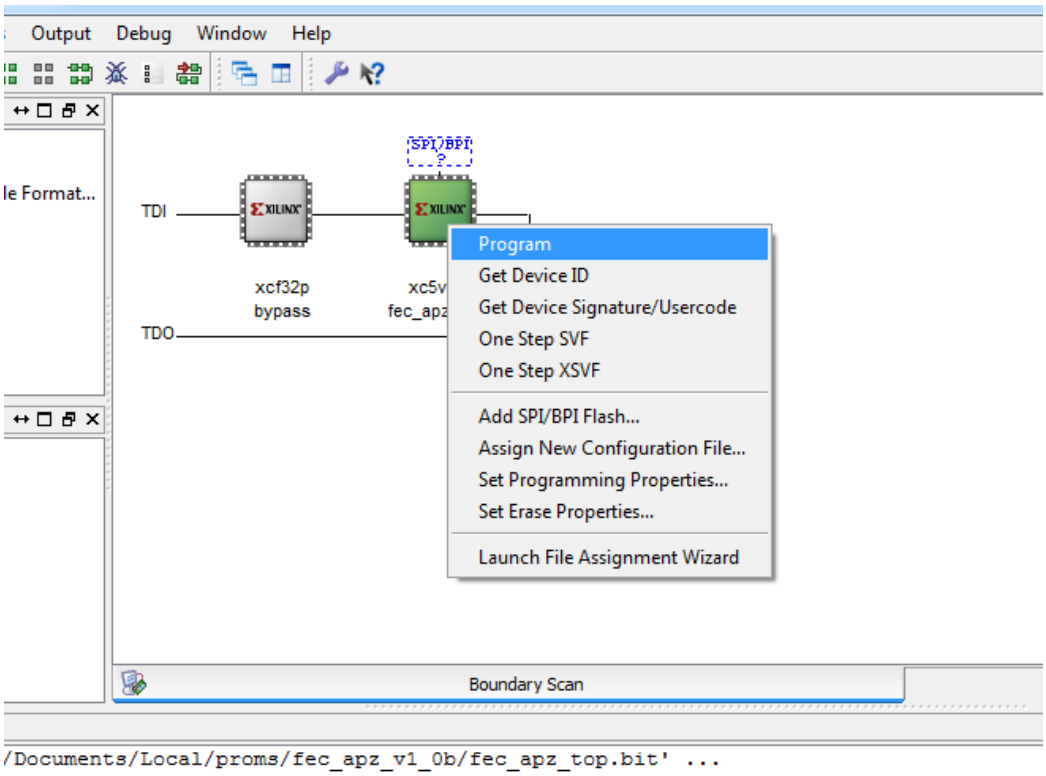
b) In the new dialog, select the *.bit* file corresponding to the new firmware from the location where you unpacked the zip file downloaded from the web.



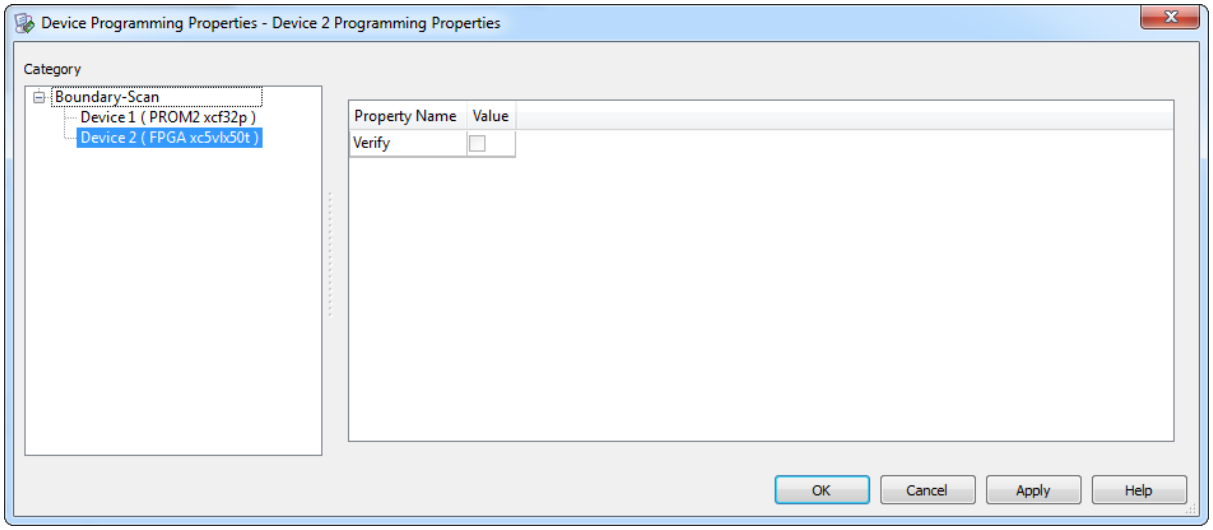
c) Press *No* when asked to attach a SPI or BPI PROM



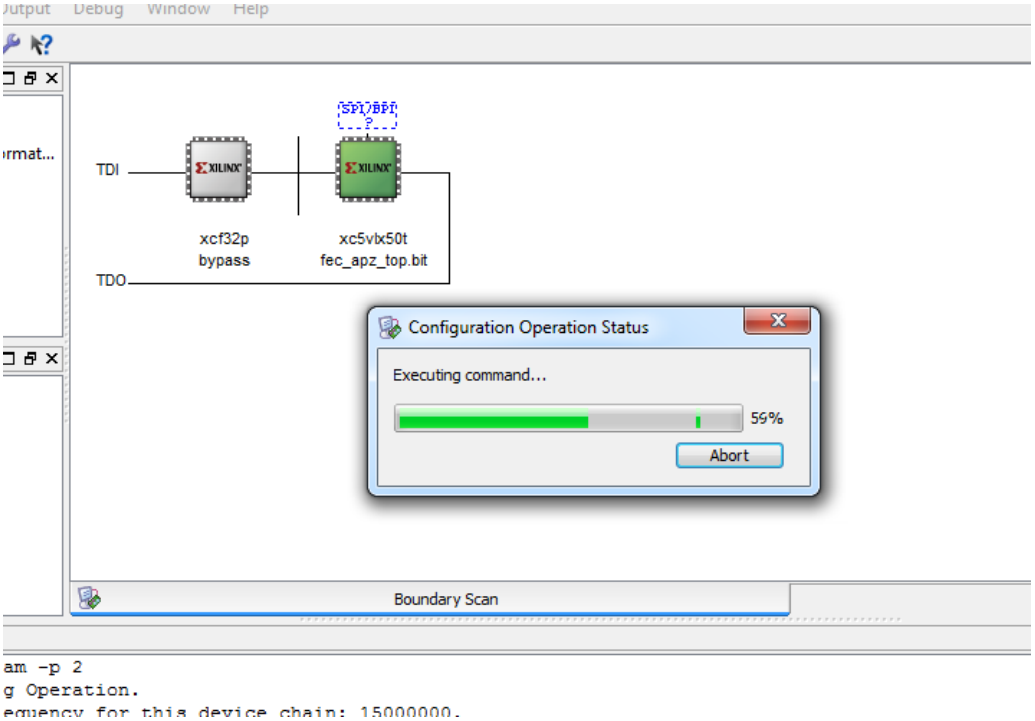
d) Right-click again on the FPGA device and select *Program*



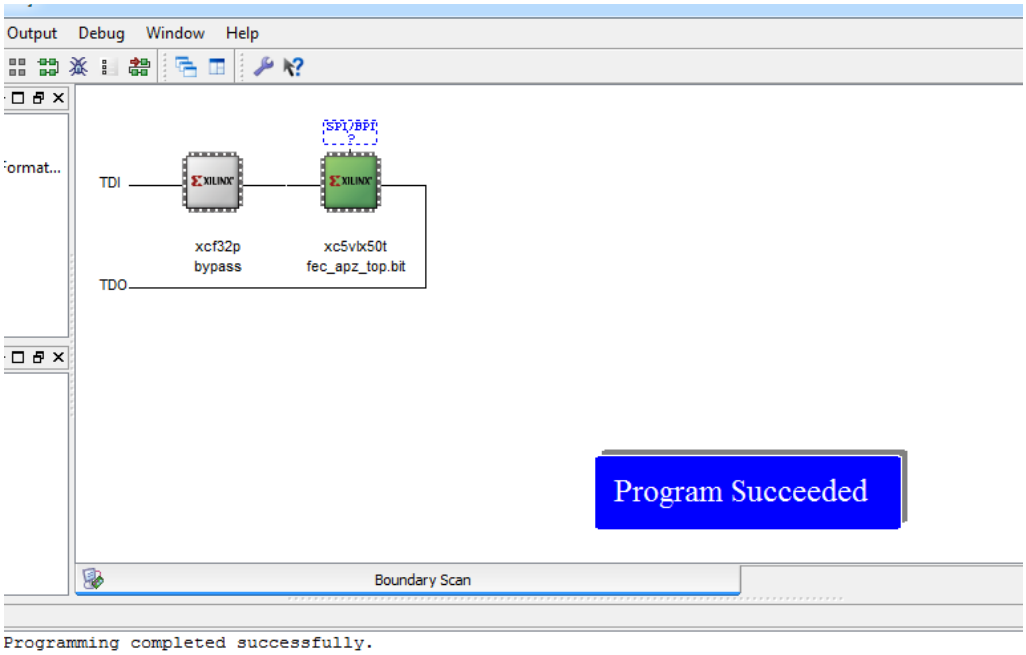
e) Click *OK* to accept the default programming properties



f) Wait until Impact loads the firmware to the FPGA

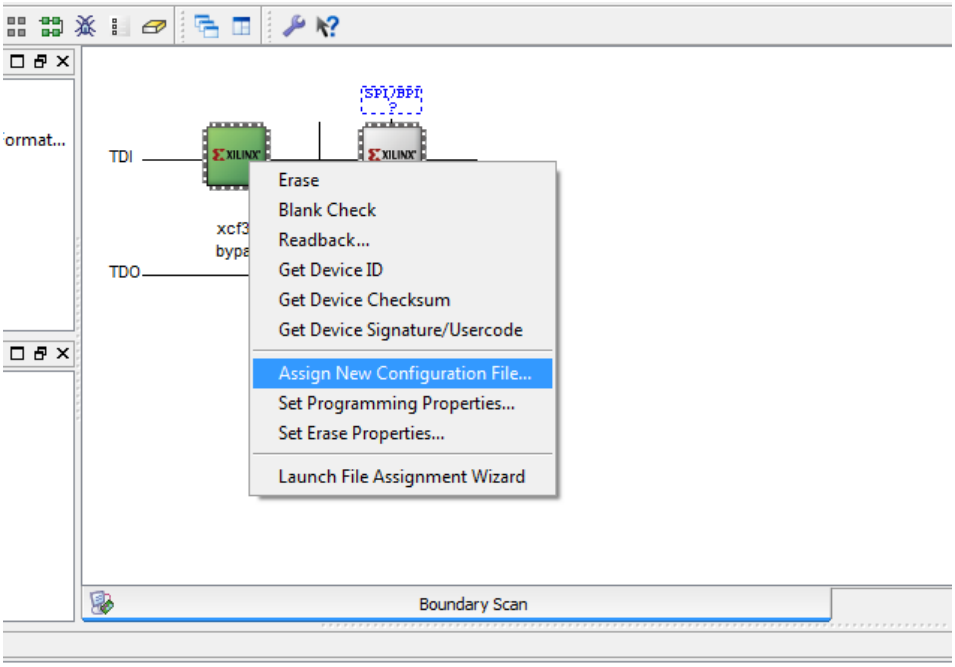


g) If the programing procedure was successful Impact will display “Program Succeeded”. You can now use the new firmware. Remember that the FPGA will revert to the old firmware after a power cycle or reboot command.

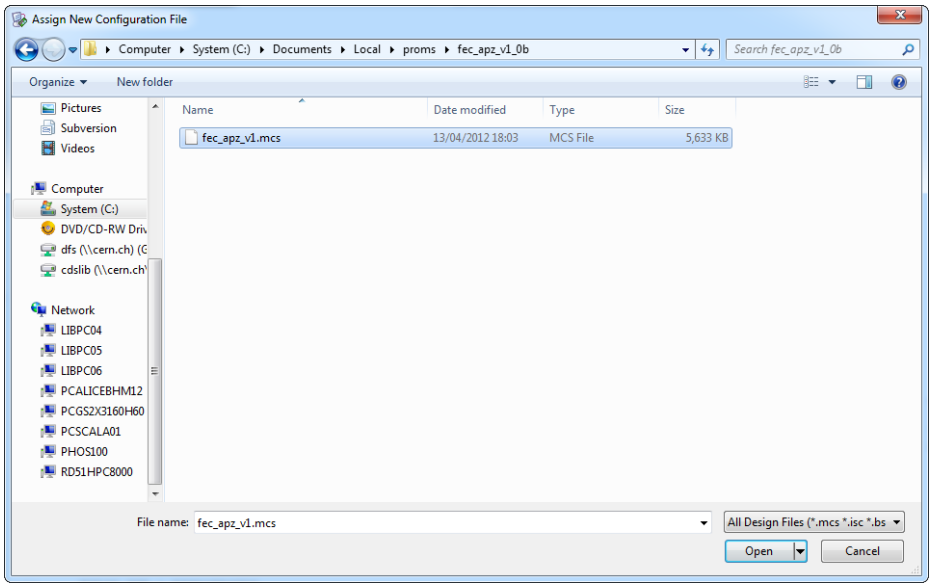


1.3.2 Program the on-borard boot EEPROM (permanent programming)

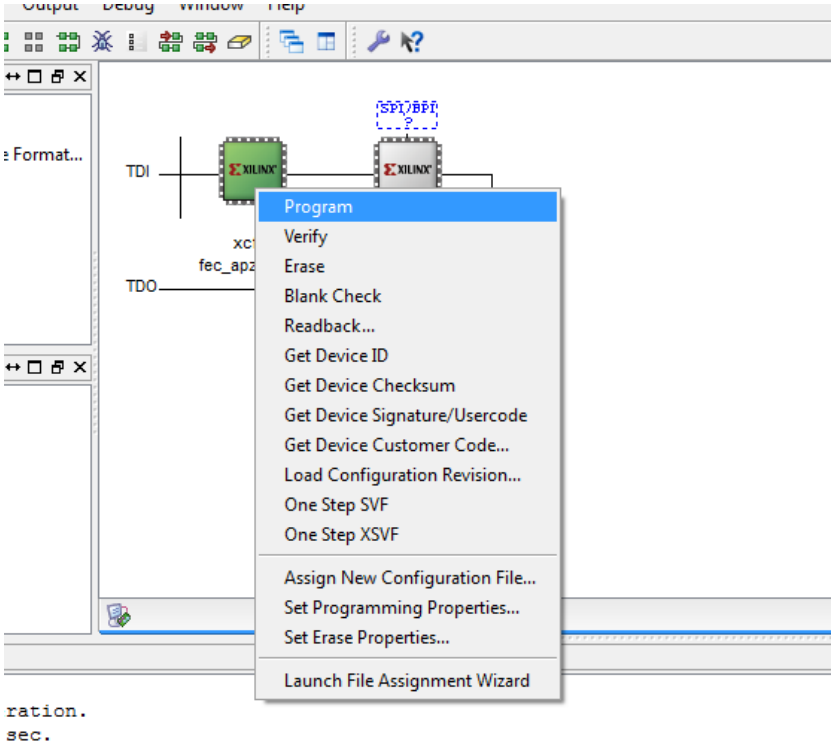
a) On the Boundary Scan tab right-click on the EEPROM device (xcf32pt) and select *Assign New Configuration File …*



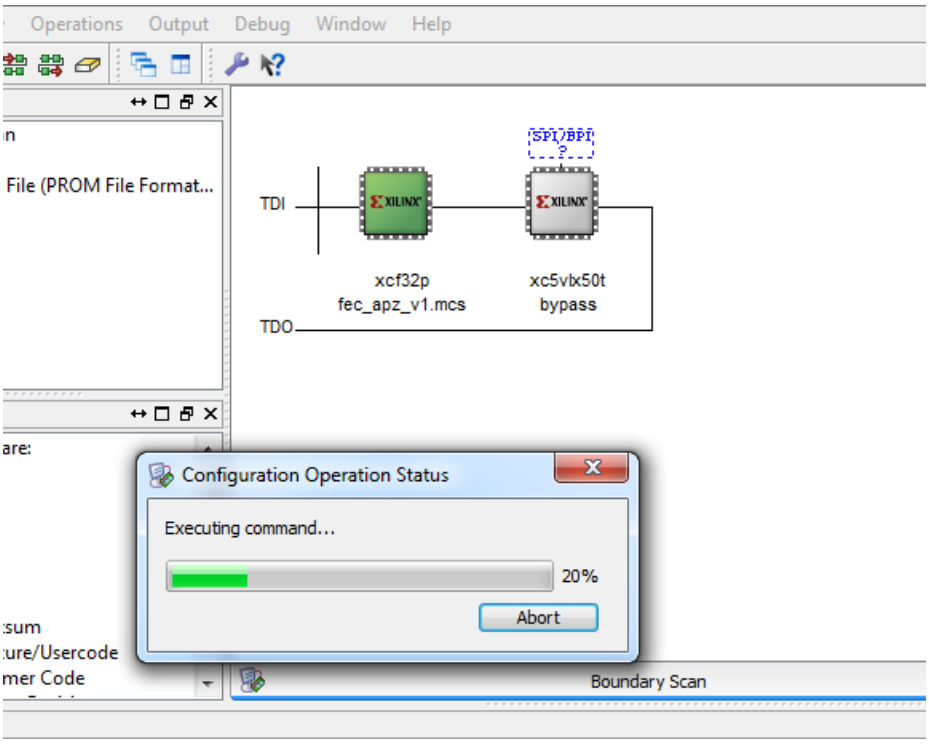
b) In the new dialog, browse to the location where you unpacked the zip file downloaded from the web and select the *.mcs* file corresponding to the new firmware.



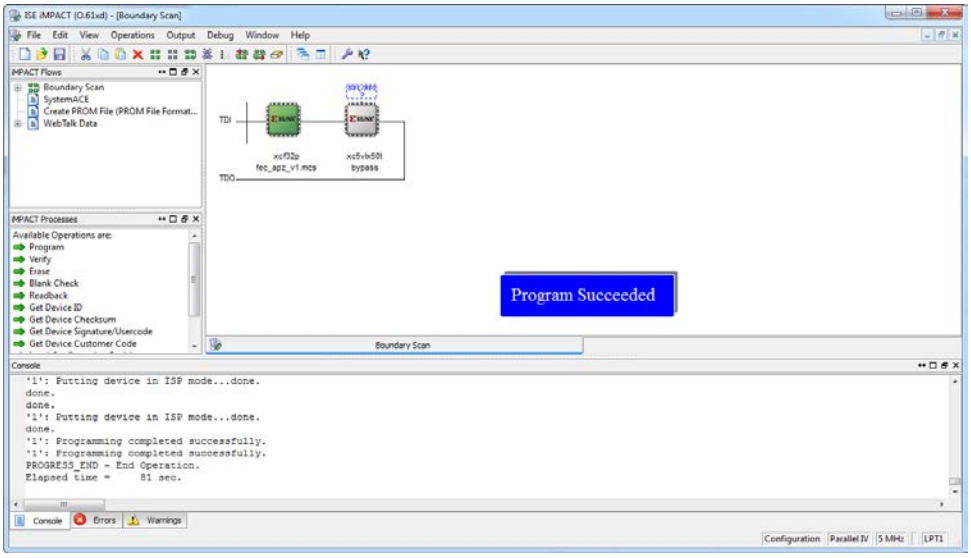
c) Right-click again on the EEPROM device and select *Program*



d) Wait until Impact loads the firmware to the EEPROM



e) If the programing procedure was successful Impact will display “Program Succeeded”. You can now power cycle the FEC board to load the new firmware from the boot EEPROM.


ISE iMPACT (O.61xd) - [Boundary Scan]
File Edit View Operations Output Debug Window Help
iMPACT Flows
Boundary Scan
SystemACE
Create PROM File (PROM File Format...
WebTalk Data
iMPACT Processes
Available Operations are:
Program
Verify
Erase
Blank Check
Readback
Get Device ID
Get Device Checksum
Get Device Signature/Usercode
Get Device Customer Code
TDI
TDO
xcf32p
fec_apz_v1.mcs
xc5vlx50t
bypass
Program Succeeded
Boundary Scan
Console
'1': Putting device in ISP mode...done.
done.
done.
'1': Putting device in ISP mode...done.
done.
'1': Programming completed successfully.
'1': Programming completed successfully.
PROGRESS_END - End Operation.
Elapsed time = 81 sec.
Console
Errors
Warnings
Configuration
Parallel IV
5 MHz
LPT1