FEC Firmware Upgrade Tutorial

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1 FEC programming using the Xilinx Impact software

1.1 Installing the Xilinx Impact software

Go to the Xilinx.com website section Products -> Design Tools and download and install the free ISE WebPACK. If you have access to a full installation package (eg. CERN dfs) you can install the "Lab Tools" only, which will install Impact without the need to purchase or request a licence. The Xilinx software supports both Linux and Windows platforms.



You will also need to use the Xilinx Programmer cable (Platform Cable USB II)

You can find more information about alternative programming options from the Xilinx website, in the <u>Products – Technology - Configuration Solutions</u> section. In particular Digilent offers programming solutions compatible with the Xilinx software (for more details go to <u>http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,395&Cat=5</u>)

1.2 Connecting the Xilinx programming dongle to the FEC card

- a) Connect the Xilinx Programmer to the PC and wait until it is recognized and the corresponding drivers are automatically installed (Windows)
- b) Make sure the FEC card is switched off, then connect the flat cable of the Xilinx Programmer to the corresponding FEC connector (U15)



c) Power on the FEC card. If power conditions are ok, the light on the Xilinx Programmer will turn green.

1.3 Programming the FEC board

a) Start the Impact software from the Start Menu:



b) Answer Yes when asked to create a project



c) Make sure that ... Boundary-Scan (JTAG) is selected and press OK

Please select an action from the list below							
Configure devices using Boundary-Scan (JTAG)	Configure devices using Boundary-Scan (JTAG)						
Automatically connect to a cable and identify Boundary-Scan chain 💌							
Prepare a PROM File							
Prepare a System ACE File							
Prepare a Boundary-Scan File							
SVF 👻							
OK							

d) The program will automatically identify the devices EEPROM and FPGA devices present on the FEC JTAG chain. Press *No* when asked to automatically assign configuration files.

SE IMPACT (0.61xd) - [Boundary Scan]	_ 0 _ X
🕼 File Edit View Operations Output Debug Window Help	- 8 ×
MPACT Flows $\leftrightarrow \Box \ \vec{\sigma} \times \mathbb{R}$ Ruht click device to select operations	
Image: System ACE System ACE Image: Create PROM File (PROM File Format Image: System ACE Image: Image: Create PROM File Promat Image: System ACE Image: Image: Image: Create PROM File Promat Image: System ACE Image: Image	
MPACT Processes $\leftrightarrow \Box \ \partial \times$	
Available Operations are: Auto Assign Configuration Files Query Dialog Do you want to continue and assign configuration files(s)? Don't show this message again, save the setting in preference. Yes No Boundary Scan	
Consoe © INFO:IMPACT:1777 - Reading C:/EDA/X11nx/v13_2/ISE_DS/ISE/xcfp/data/xcf32p.bsd © INFO:IMPACT:501 - '1': Added Device xcf32p successfully. 	
PROGRESS_END - End Operation. Elapsed time = 0 sec. // *** BATCH CMD : identifyMPM 	*
Configuration Parallel IV 5 M	Hz LPT1

e) Press OK to accept the default programming parameters

Device Programming Properties - Device 1 Programming Properties							
Category							
Device 1 (PROM2 xcf32p)	Property Name	Value					
Device 2 (FPGA xc5vlx50t)	Verify						
	General CPLD And PROM Properties						
	Design-Specific Erase Before Programming						
	Read Protect						
	PROM/CoolRunner-II Usercode (8 Hex Digits)						
	PROM Specific Properties						
	Load FPGA						
	Parallel Mode						
	Advanced PROM Programming Properties						
	During Configuration: PROM is Configuration Master (check to select clock source)						
	[select clock source]	External Clock 👻					
	During Configuration: PROM is Slave (clocked externally)						
	OK	Cancel Apply Help					

1.3.1 Temporarily programming the FEC FPGA

The firmware can be loaded directly into the FPGA without writing it permanently to the on-board EEPROM. This operation is useful for testing a new firmware update with minimum risk. At the next power cycle, the FPGA will boot with the default firmware stored on the local EEPROM. If you want to continue testing the new firmware you need to reload it to the FPGA.

If you want to permanently write the new firmware to the FEC board, go to next section (1.3.2 Program the on-borard boot EEPROM (permanent programming))

a) On the Boundary Scan tab right-click on the FPGA device (xc5vlx50t) and select Assign New Configuration File ...



b) In the new dialog, select the *.bit* file corresponding to the new firmware from the location where you unpacked the zip file downloaded from the web.

Assign New Configuration File							
Computer	System (C:) Documents Local pror	ms ▶ fec_apz_v1_0b		- 4 ₇	Search fec_apz_v1	_0b	٩
Organize 🔻 New folder					333	•	0
★ Favorites	Name	Date modified	Туре	Size			
Desktop	fec_apz_top.bit	12/04/2012 16:29	BIT File	1,716 K	В		
Downloads Dublic on DES							
Recent Places							
📕 SRS 📰							
smartoiu							
Ja Local							
🕞 Libraries							
Documents							
Pictures							
Subversion							
Videos							
Computer							
System (C:)							
😌 DVD/CD-RW Driv							
G dfc (\\cern ch) (6							
File nan	ne: fec_apz_top.bit			•	All Design Files (*.b	it ".rbt ".nl	sy ▼
					Open 🔻	Cance	

c) Press No when asked to attach a SPI or BPI PROM



d) Right-click again on the FPGA device and select Program



/Documents/Local/proms/fec_apz_v1_0b/fec_apz_top.bit' ...

e) Click OK to accept the default programming properties

Bevice Programming Properties - Device 2	Programming Properties	x
Category		
Device 1 (PROM2 xcf32p)	Property Name Value	
	Verify	
	OK Cancel Apply H	Help



f) Wait until Impact loads the firmware to the FPGA

equency for this device chain: 15000000.

g) If the programing procedure was successful Impact will display "Program Succeeded". You can now use the new firmware. Remember that the FPGA will revert to the old firmware after a power cycle or reboot command.



Programming completed successfully.

1.3.2 Program the on-borard boot EEPROM (permanent programming)

a) On the Boundary Scan tab right-click on the EEPROM device (xcf32pt) and select Assign New Configuration File ...



b) In the new dialog, browse to the location where you unpacked the zip file downloaded from the web and select the *.mcs* file corresponding to the new firmware.

Assign New Configuration File								
🚱 🕞 🖉 🖟 Computer > System (C:) > Documents > Local > proms > fec_apz_v1_0b 🔹 🚽 Search fec_apz_v1_0b								م
Organize 🔻 New fo	lder					!≡ ▼		0
Pictures	•	Name	Date modified	Туре	Size			
Subversion		fec_apz_v1.mcs	13/04/2012 18:03	MCS File	5,633 KB			
Videos								
🖳 Computer								
🏭 System (C:)								
🙂 DVD/CD-RW Driv								
dfs (\\cern.ch) (C								
Casilo (//cem.ch								
👊 Network								
IIBPC04								
🖳 LIBPC05								
IBPC06	=							
PCALICEBHM12								
PCG32X3100H00								
PHOS100								
PRD51HPC8000								
	-							
File	e nam	e: fec_apz_v1.mcs			- AI	I Design Files (*.mcs *.	isc *.bs	•
						Open 🚽	Cancel	
						(·		

c) Right-click again on the EEPROM device and select Program



d) Wait until Impact loads the firmware to the EEPROM

Outputient Output	Debug Mündere Hele
Operations Output	Debug Window Heip
# # 🖉 📑 🔳	/ k?
↔□₽×	
n	(SPI)BPI
	(?)
File (PROM File Format	
	xcf32p xc5vlx50t
	fec_apz_v1.mcs bypass
	TDO

↔□₽×	
are:	
🛛 🐼 Confi	guration Operation Status
Executir	ig command
	2086
	2078
sum	Abort
:ure/Usercode	
mer Code 🔍 👻	Boundary Scan

e) If the programing procedure was successful Impact will display "Program Succeeded". You can now power cycle the FEC board to load the new firmware from the boot EEPROM.

BE IMPACT (0.61xd) - [Boundary Scan]		
File Edit View Operations Output	Debug Window Help	- 7 ×
	1 B B B B B P R	
MPACT Plans ··· □ # ×		
	TDI Example sc02p sc04001 fec.upt_v1.ncs byses	
MPACT Processes **		
Available Operations are:	Program Succeede	d
Console		+D.6 x
11: Porting device in ISP modene. done. 11: Porting device in ISP modene. 11: Programming completed sur 11: Programming completed sur 12: Programming completed sur 13: Programming completed sur 14: Programming	edone. done. ceastully. ceastully.	
CONTROL FILLS SUCCESS		