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Calculation and Measurement of the Interstrip Capacitance and its Correlation With Measured ENC for the GE2/1 GEM Detector

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Abstract

Proposed for the Phase 2 upgrade of the muon detectors for the CMS experiment, the GE2/1 GEM detector will be installed in the muon endcap to account for the increased trigger rates resulting from the increased luminosity after the high luminosity LHC upgrade. As with any detector, a high signal-to-noise ratio is desirable, and the noise is a function of the capacitance between adjacent readout strips on the readout board. This internal note reports on the analytical calculations and the physical measurements of this interstrip capacitance taken for 12 different strip geometries and dimensions on a custom-built GE2/1 prototype readout board. Interstrip capacitance measurements were taken for two different configurations: (1) with a copper-covered printed circuit board plate suspended 1 mm from the readout board, which simulated the capacitance contribution from the bottom of the third GEM foil, and (2) without the presence of the plate. Equivalent noise charge measurements are presented and compared with the corresponding interstrip capacitance measurements. The lowest measured interstrip capacitance without the presence of the copper-covered printed circuit board in the M1 module results from halving the original strip length, and from doubling the original width and halving the original strip length in the M4 module. With the addition of the copper-covered printed circuit board, we find on average an increase of about 15% in the interstrip capacitance. We also observe a linear correlation between measured ENC and measured interstrip capacitance. The agreement between the analytical calculations and the measured interstrip capacitance is about 20-30%.

1 Introduction

The proposed High Luminosity LHC (HL-LHC) upgrade will result in an increase of the integrated luminosity by an order of magnitude [1]. As a consequence of this increased luminosity, muon trigger rates will increase as well. One of the proposed detectors for the Phase 2 upgrade of the CMS muon detectors, which will help cope with the increased trigger rates, is the GE2/1 gas electron multiplier (GEM) detector, which will be placed in tandem with the cathode strip chambers (CSC) ME2/1. These detectors will be placed in the endcap, in addition to the recently constructed GE1/1 detectors, and will serve to increase redundancy and form another measure of muon direction and momentum at L1 trigger level [1].

Maximizing the signal-to-noise (S/N) in a detector is an important design goal, and it is known that the interstrip capacitance of the strips on the readout board (ROB) of a detector directly influence the noise. Because capacitance is a function of the geometry and dimensions of the conductors in a system, modifying the dimensions and geometrical parameters of the strips can successfully reduce the interstrip capacitance, which will consequently reduce the noise. This note will report on both the analytical calculations used to approximate the interstrip capacitance of different strip geometries and dimensions, as well as the physical measurements of the interstrip capacitance of a custom-built GE2/1 prototype ROB. Additionally, equivalent noise charge (ENC) measurements will be presented and correlated with the interstrip capacitance of different strip designs.

2 Calculation and Measurement of the Interstrip Capacitance of the GE2/1

2.1 Layout and Design of the GE2/1 Readout Board

The custom GE2/1 ROB was designed so that different strip dimensions and geometries proposed for the M1 and M4 modules, i.e. the smallest and the largest module, respectively, in the GE2/1 detector could be placed on a GE1/1 ROB (see [2] for more details). Different strip designs were implemented in twelve separate sectors on this custom GE2/1 ROB. Here ”strips” refers to the readout strips on the ROB side that faces the GEM foils and ”traces” refers to the signal lines on the other side of the ROB that connects the strips to the readout connector. These designs are listed below in Tab. 1, and shown in Fig. 1:

Table 1: GE2/1 ROB Layout

Sector	Module	Modified Parameter(s)
1	**M4**	Original TDR design (Strip Gap: 0.2 mm)
2	**M4**	Strip Gap: 0.3 mm
3	**M4**	Doubled Strip Width, Halved Strip Length
4	**M4**	Original TDR Design with Long traces
5	**M1**	Original TDR Design (Strip Gap: 0.2 mm)
6	**M1**	Strip Gap: 0.3 mm
7	**M1**	Strip Gap: 0.4 mm
8	**M1**	Doubled Strip Width, Halved Strip Length
9	**M1**	Halved Strip Length
10	**M1**	Original TDR Design with Long traces
11	**M1**	Original TDR Design with Minimal traces
12	**M1**	Minimal traces, Halved Strip Length, Doubled Strip Width

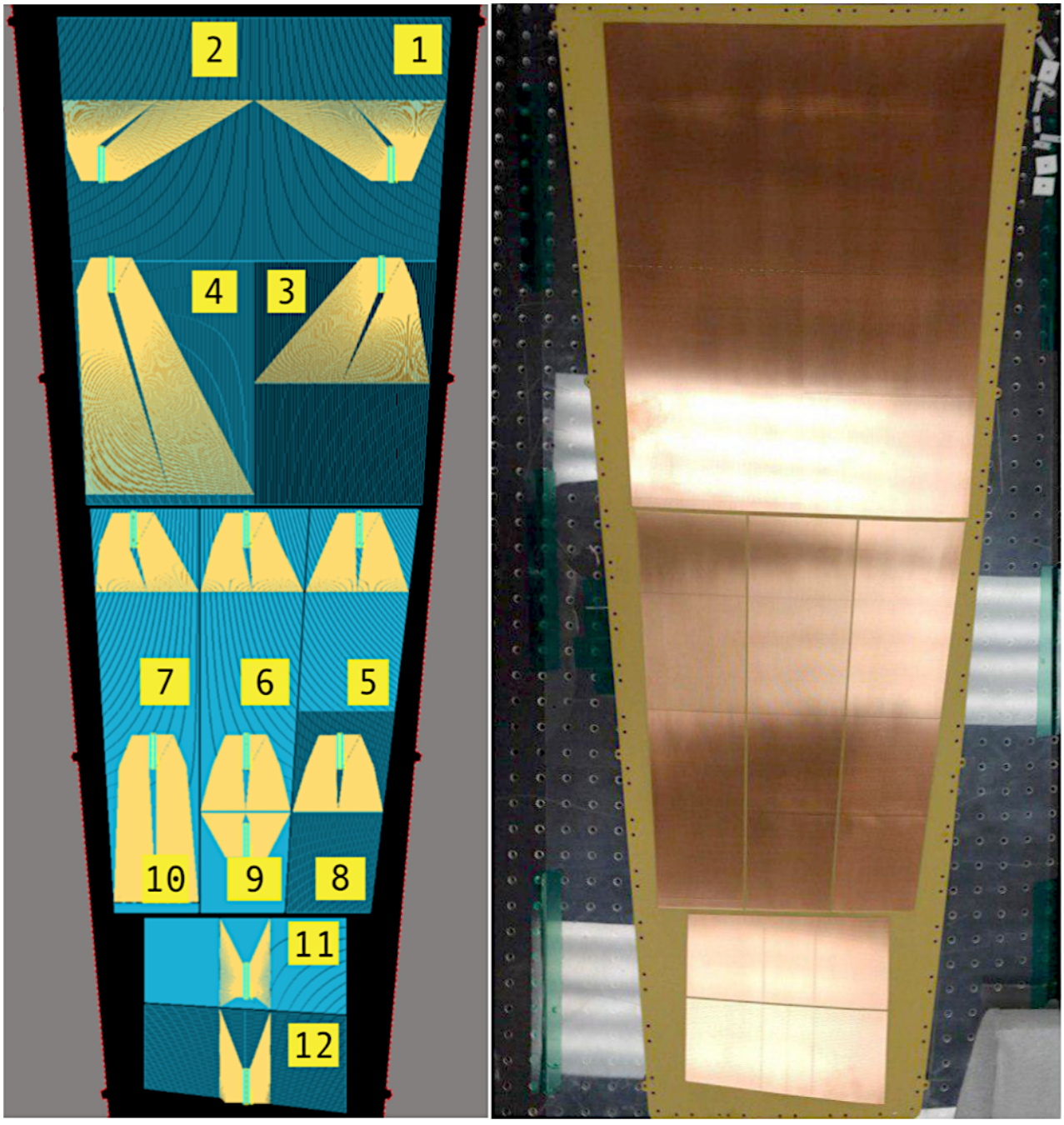

Figure 1: Diagram of the layout of the GE2/1 custom ROB (left) and a photo of the readout strip side of this board where measurements were taken (right). The figure on the left indicates the trace routing and the position of the readout connector (green) and was adapted from [2].

2.2 Analytical Calculation of the Interstrip Capacitance

The interstrip capacitance per centimeter of strip length on the readout board of the GE2/1 chamber is calculated using a modified version of the equation presented in [3], which was obtained through a series of conformal transformations of two co-planar strips on a dielectric substrate. In previous work [4], the original expression in [3] was used, which yielded a discrepancy between calculation and measurement of about 60-80%. Here, the original expression was modified to include an extra term to account for both the readout strips on the front side of the board and the signal traces on the other side of the board that run to connectors for the front-end electronics on the ROB. Fig. 2 displays the geometry of the modeled system. Equations (1)-(5) below were used to calculate the interstrip capacitance of the composite strip, trace, and substrate system. Equation (1) is the linear sum of the strip/substrate system and the trace/substrate system, where C_a is the capacitance per centimeter between the strips with air above and below, C_{sa} is the additional capacitance between the strips due to the presence of the substrate below them, C_t is the interstrip capacitance per centimeter of the traces with air above and below them, and C_{st} is the additional capacitance between the traces due the the presence of the substrate.

$$(C/l) = \big(C_{sa}+C_a\big)l_s^{-1}+\big(C_{st}+C_t\big)l_t^{-1} = \epsilon_0\left((\epsilon-1)\frac{K(k')}{2K(k)}+\frac{K(k'_0)}{K(k_0)}\right)+\epsilon_0\left((\epsilon-1)\frac{K(k'_t)}{2K(k_t)}+\frac{K(k'_{0t})}{K(k_{0t})}\right) \quad (1)$$

where

$$k = \tanh\left(\frac{\pi g}{2h}\right)\coth\left(\frac{\pi(w+g)}{2h}\right), \qquad k' = \sqrt{1-k^2} \quad (2)$$

$$k_0 = \frac{g}{w+g}, \qquad k'_0 = \sqrt{1-k_0^2} \quad (3)$$

$$k_t = \tanh\left(\frac{\pi g_t}{2h}\right)\coth\left(\frac{\pi(w_t+g_t)}{2h}\right), \quad k'_t = \sqrt{1-k_t^2} \quad (4)$$

$$k_{0t} = \frac{g_t}{w_t+g_t}, \qquad k'_{0t} = \sqrt{1-k_{0t}^2} \quad (5)$$

Equations (2)-(5) are the moduli of $K(k)$, which is the complete elliptic integral of the first kind, and where w is the strip width, $2g$ is the gap width between the strips, w_t is the trace width, $2g_t$ is the gap width between the traces, h is the thickness of the substrate (FR4 with dielectric constant $\epsilon = 4.7$), and ϵ_0 is the vacuum permittivity. Note here that in order to calculate the interstrip capacitance due to the presence of the traces, the trace lengths were measured twelve times in each sector, and the trace widths and gap widths were all measured 24 times: 12 times near the wide end where the signal traces are more spread out, and 12 times near the narrow end where they are closer together. This allowed for a calculation of an average trace width and gap width across the sector. An average of each parameter was then computed and used as the value in the calculation. All calculations were computed using `MATLAB` [5], and the function `ellipke()` was used for the complete elliptic integral of the first kind.

2.3 Measurement of the Interstrip Capacitance Without the Copper-Covered PCB

The interstrip capacitance was measured in all twelve sectors of the ROB with an Excelvan m6013 capacitance meter. To obtain an accurate measurement, the probes of the capacitance meter were placed at opposite ends of adjacent strip pairs, and held about a centimeter above the strips by one person while the meter was zeroed by another person. After zeroing, a reading was immediately taken. Four measurements were taken for each pair of strips measured, and between eight and nineteen strip pair measurements were taken in each of the twelve sectors. Fig. 3 below displays a map of which strip pairs were measured in each sector (yellow lines indicate a pair of strips that were measured). A weighted mean over all strips in a sector is calculated from the average of all trials for each individual strip and the standard deviation of the weighted mean is computed for all of the sectors.

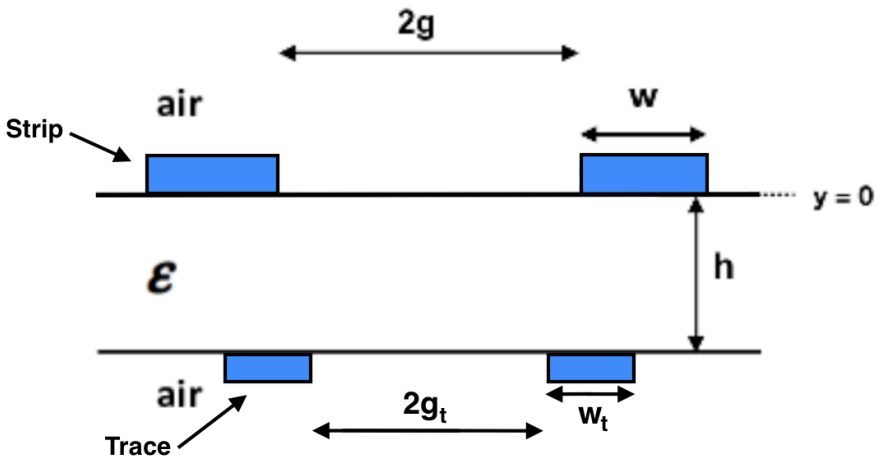

Figure 2: The readout strip and trace geometry, where w is the strip width, $2g$ is the gap width of the strips, w_t is the trace width, $2g_t$ is the gap width of the traces, and h is the thickness of the substrate with dielectric constant ϵ. Figure adapted from [4]. Note that strips and traces are connected by vias (not shown), which are conductive connections that run between the layers of the PCB.

2.4 Measurement of the Interstrip Capacitance with the Copper-Covered PCB

The interstrip capacitance for each of the twelve sectors were measured with a copper-covered PCB suspended 1 mm away from the readout board in order to simulate the contribution to the capacitance of the bottom of the third GEM foil. Because the outer diameter of the holes in the foil are $\sim 70\,\mu$m, and this foil is held 1 mm away from the ROB, we can simulate the capacitance of this foil with a solid, conducting plane placed 1 mm away from the strips on the ROB. A grounding plate that was originally designed for use with the GE1/1 GEM detectors during the quality control tests after production was used. Because this plate was mounted on the top of the ROB, there are holes to allow for the Panasonic connectors and the gas inlet/outlet plugs to be exposed. These holes were covered with copper tape in order to approximate a continuous, conducting plane (see Fig. 4).

One millimeter dielectric spacers were made of flame-retardant glass-reinforced epoxy laminate material (FR4) and placed around the edge of the ROB, and were used to hold the ROB 1 mm away from the grounding plate (see Fig. 5). Extra spacers were also used in areas where there were no readout strips to ensure that the ROB remained planar. While the measurements without the copper-covered PCB were done by directly contacting the strips with the probes, in this case, the probes of an Excelvan m6013 capacitance meter were suspended about 5 mm above the exposed traces which lead into the Panasonic connector. One person then zeroed the meter. After the meter was properly zeroed, another person contacted the adjacent trace pairs, and a measurement was recorded. This process was repeated for every single strip pair previously measured with no copper-covered PCB present (see Fig. 3 for an exact mapping of what strips were measured; note that three additional measurements were taken in sector 1).

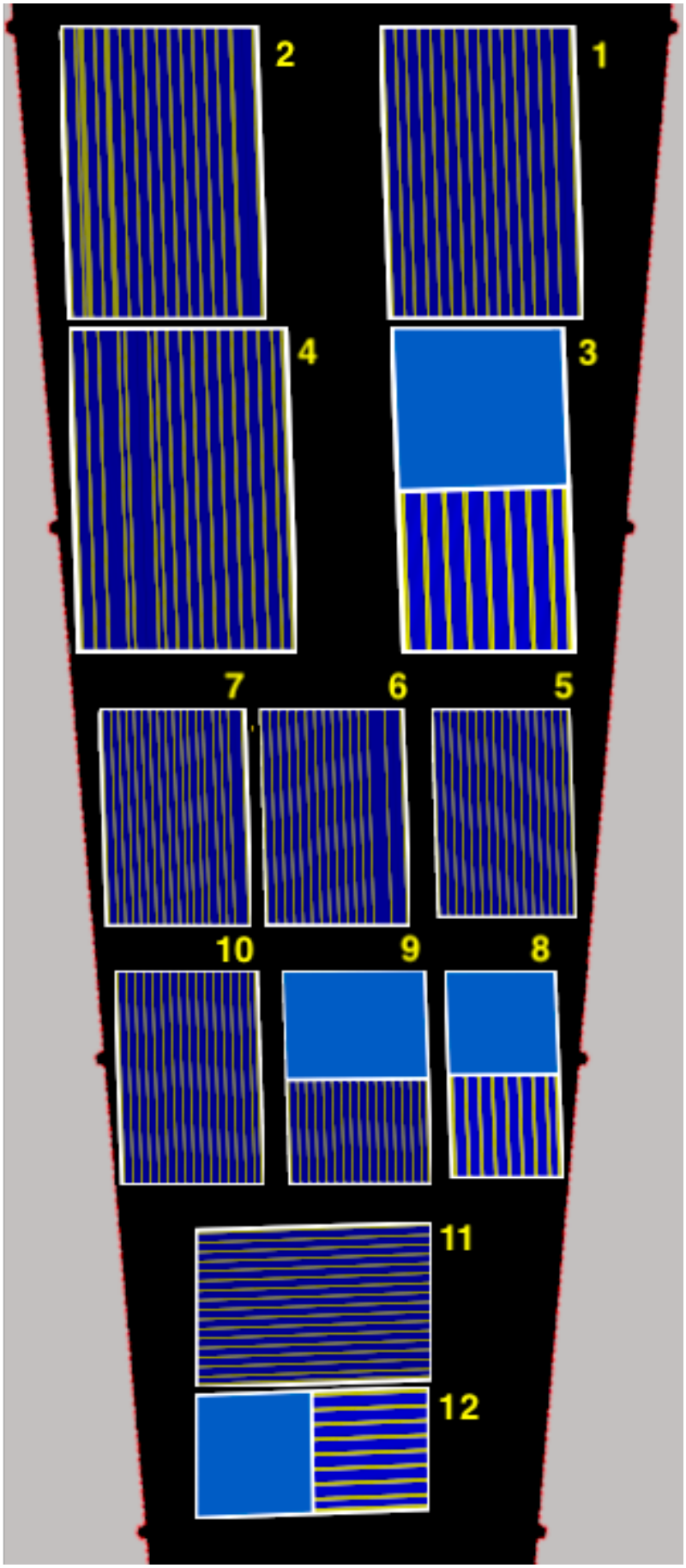

Figure 3: Map of the strip pairs which were measured in each sector (single yellow lines indicate which strip pairs were measured).

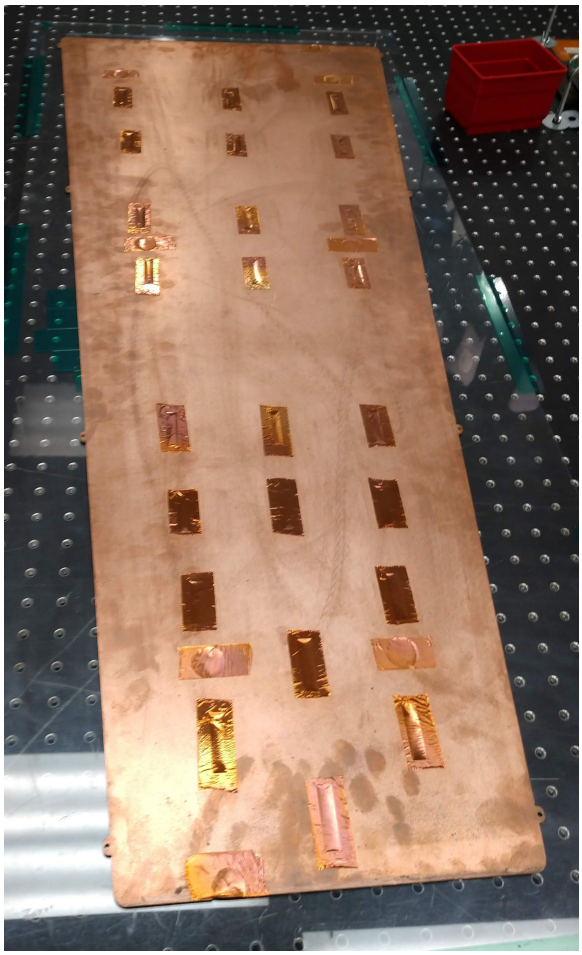

Figure 4: The GE1/1 grounding plate with the Panasonic and gas inlet/outlet plug holes covered with copper tape used to simulate the presence of the GEM foil.

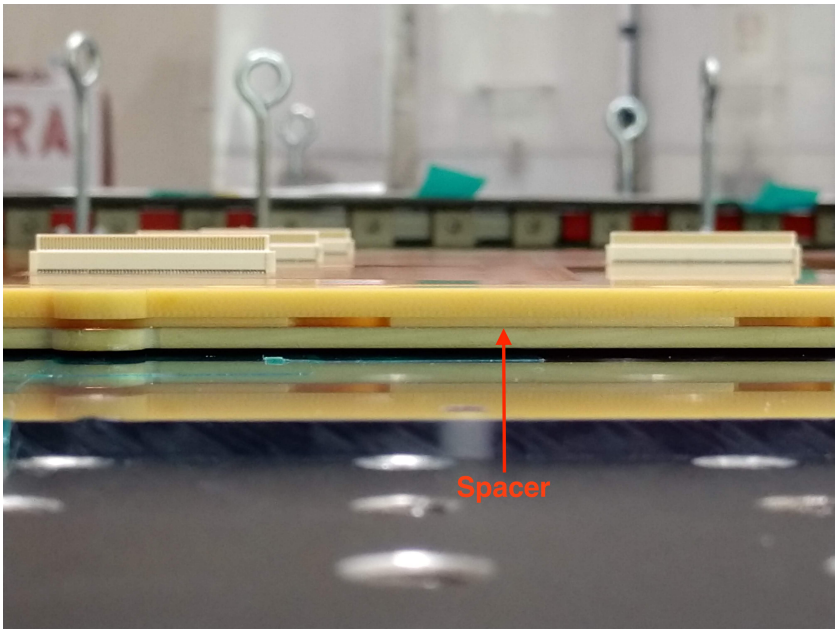

Figure 5: The custom GE2/1 ROB suspended above the copper-covered PCB using 1 mm FR4 spacers.

2.5 Results: Interstrip Capacitance Without the Copper-Covered PCB

The interstrip capacitance of the twelve different strip geometries for the M1 and M4 modules are presented. As mentioned in section 2.3, the measurements quoted are the weighted averages over all of the measured strips in the sector and the uncertainties are the standard deviations of the weighted means. The interstrip capacitance was calculated using maximum strip lengths $L_{M4} = 20.6$ cm and $L_{M1} = 19.6$ cm, and the trace dimensions listed in Tab. 2. Tab. 3 below displays the measurements and the calculations for each of the sectors, and the ratio of the measured capacitance to the calculated capacitance.

Table 2: GE2/1 ROB Trace Dimensions

Sector	Module	Parameters	Avg. Meas. Length (cm)	Avg. Meas. Width (mm)	Avg. Meas. Gap Width (mm)
1	M4	Original TDR design (Strip Gap: 0.2 mm)	8.490 ± 1.796	0.48 ± 0.02	0.67 ± 0.02
2	M4	Gap: 0.3 mm	9.234 ± 1.916	0.38 ± 0.02	0.72 ± 0.06
3	M4	2×Width, 0.5×Length	10.93 ± 1.59	0.44 ± 0.01	0.76 ± 0.05
4	M4	Long traces	21.95 ± 0.91	0.38 ± 0.01	0.66 ± 0.02
5	M1	Original TDR design (Strip Gap: 0.2 mm)	6.140 ± 1.122	0.60 ± 0.03	0.44 ± 0.03
6	M1	Gap: 0.3 mm	5.438 ± 0.957	0.41 ± 0.01	0.59 ± 0.03
7	M1	Gap: 0.4 mm	5.576 ± 1.027	0.39 ± 0.01	0.47 ± 0.03
8	M1	2×Width, 0.5×Length	6.209 ± 1.136	0.34 ± 0.01	0.45 ± 0.01
9	M1	0.5×Length	1.990 ± 0.979	0.35 ± 0.02	0.51 ± 0.18
10	M1	Original TDR design, Long traces	13.00 ± 0.07	0.33 ± 0.01	0.43 ± 0.01
11	M1	Original TDR design, Minimal traces	3.425 ± 0.741	0.38 ± 0.01	0.40 ± 0.05
12	M1	Minimal traces, 0.5×Length, 2×Width	3.806 ± 1.227	0.38 ± 0.01	0.45 ± 0.08

Table 3: GE2/1 ROB Interstrip Capacitances For Open ROB

Sector	Module	Parameters	Avg. Meas. Cap. (pF)	Calc. Cap. (pF)	Meas. Cap. / Calc. Cap.
1	M4	Original TDR design (Strip Gap: 0.2 mm)	21.69 ± 0.05	16.7	1.30
2	M4	Gap: 0.3 mm	19.98 ± 0.12	15.3	1.31
3	M4	2×Width, 0.5×Length	15.32 ± 0.03	10.5	1.46
4	M4	Long traces	27.87 ± 0.09	21.1	1.32
5	M1	Original TDR design (Strip Gap: 0.2 mm)	16.27 ± 0.04	12.7	1.28
6	M1	Gap: 0.3 mm	14.65 ± 0.07	11.2	1.31
7	M1	Gap: 0.4 mm	13.17 ± 0.04	10.6	1.24
8	M1	2×Width, 0.5×Length	11.82 ± 0.06	8.5	1.39
9	M1	0.5×Length	9.32 ± 0.05	5.9	1.58
10	M1	Original TDR design, Long traces	20.07 ± 0.07	15.3	1.31
11	M1	Original TDR design, Minimal traces	14.02 ± 0.02	11.8	1.19
12	M1	Minimal traces, 0.5×Length, 2×Width	10.39 ± 0.07	7.6	1.37

As expected, the trace length influences the interstrip capacitance. Comparing the average measured interstrip capacitance of the default configuration of the M4 module (sector 1) with the default configuration of the M4 module but with long traces (sector 4), one can see that the interstrip capacitance is around 6 pF higher, which is about 30% larger in both the measured and calculated interstrip capacitance. The same effect can be seen when comparing the default strip configuration of the M1 module (sector 5) with the default strip configuration of the M1 module with long traces (sector 10); the configuration with extra long traces is about 4 pF larger ($\sim 23\%$ larger). Similarly, the interstrip capacitance of the default M1 module (sector 11) configuration with minimal traces, when compared with the default M1 module, is about 2 pF lower ($\sim 16\%$ smaller). From these measurements, it can be concluded that the trace length on the ROB is a critical design parameter that should be minimized.

Overall, the configurations with the lowest interstrip capacitance, both calculated and measured, are the M4 module with doubled strip width and halved strip length, sector 3 ($C = 15.32 \pm 0.03$ pF), and the M1 module with the strip lengths halved, sector 11 ($C = 9.32 \pm 0.05$ pF). This shows about a 29% reduction of the interstrip capacitance in the M4 module relative to the original design in the muon upgrade technical design report (TDR) [1], and about a 43% reduction of the interstrip capacitance in the M1 module relative to the original TDR design. We can also

see that the calculations scale roughly with the same proportions as the measurements do (with respect to comparing the new values to the original TDR design configurations). For instance, when comparing the percentage of reduction of interstrip capacitances of sector 3 compared to sector 1, there is about a 10% discrepancy between the relative reduction in the calculated interstrip capacitance and the measured capacitance (i.e., comparing the ratio of the calculated interstrip capacitance of sector 1 to 3 and the ratio of the measured interstrip capacitance for these sectors). Most sectors show about a 10% discrepancy, while the largest discrepancy is 23%. Because the calculations scale in roughly the same proportions as the measurements, we can conclude that the calculations do indeed reflect the behavior of the interstrip capacitance as the various parameters of the strip configurations are changed. In general, we can conclude from both the calculations and the measurements that altering the gap width produces the least change in interstrip capacitance, and that altering the lengths and the width of the strips produces the largest decrease in interstrip capacitance.

Another important point is that calculations presented in a previous note [4] were performed without the additional term for the trace/substrate system. By including this extra term, the discrepancy between the average measured interstrip capacitance and the calculated capacitance was lowered from about 60-80% to around 30% on average, which indicates that including the capacitance contribution from the trace/substrate system results in a more accurate approximation. This discrepancy arises from the simplified model used to calculate the interstrip capacitance; the analytical expression only considers two adjacent strips with two signal traces on the other side of the ROB, whereas the actual configuration has 128 strips/signal traces per sector, and so the influence of these additional conductors is not considered in the calculations. This discrepancy between calculation and measurement also provides the motivation for directly measuring the interstrip capacitance with the presence of an opposing conductor, which will simulate the capacitance contribution for GEM3 bottom. In reality, the ROB will be held 1 mm away from the bottom of the third GEM foil, and so this approximation will help provide a more realistic value of the interstrip capacitance when the ROB is fixed to the chamber. These interstrip capacitance measurements with the addition of a copper-covered PCB are presented in the following section 2.6.

2.6 Results: Interstrip Capacitance With the Copper-Covered PCB

The average interstrip capacitance both with and without the presence of the copper-covered PCB, and the ratio of the two are presented for each sector of the ROB in Tab. 4. In the M4 module, with doubled width and halved strip length, the interstrip capacitance is reduced by 29% compared to the original TDR design; in the most realistic case (with the presence of the third GEM foil simulated by the copper plate), the interstrip capacitance is reduced by 22%. For the M1 module with halved length, the interstrip capacitance is reduced by 43%; with the simulated presence of the third GEM foil, we see a 50% reduction in the interstrip capacitance. One can immediately see that the interstrip capacitance is increased with the presence of the copper plate. On average, the interstrip capacitance increases by $\sim 15\%$. Several interesting trends are also present in these data. First, the ratio of the capacitances with and without the simulated third GEM foil in sectors with long traces (sectors 3 and 10) each increase by about 30%. Second, the interstrip capacitances of the default strip configurations, for both the M1 and M4 module strip designs increase with roughly the same proportion ($\sim 18\%$) when the copper plate is added. In Fig. 6 below, the

Table 4: GE2/1 ROB Interstrip Capacitance With and Without Grounding Plate

Sector	Module	Parameters	Avg. Meas. Cap. w/o plate (pF)	Avg. Meas. Cap. w/plate (pF)	$(C_w/C_{w/o})$
1	M4	Original TDR design (Strip Gap: 0.2 mm)	21.69±0.05	25.85±0.27	1.192±0.013
2	M4	Gap: 0.3 mm	19.98±0.12	20.98±0.03	1.050±0.006
3	M4	2×Width, 0.5×Length	15.33±0.03	20.16±0.04	1.315±0.004
4	M4	Long traces	27.87±0.06	28.43±0.07	1.020±0.003
5	M1	Original TDR design (Strip Gap: 0.2 mm)	16.27±0.04	19.04±0.21	1.170±0.013
6	M1	Gap: 0.3 mm	14.65±0.07	18.26±0.06	1.246±0.007
7	M1	Gap: 0.4 mm	13.17±0.04	14.85±0.08	1.128±0.007
8	M1	2×Width, 0.5×Length	11.82±0.06	15.82±0.32	1.338±0.028
9	M1	0.5×Length	9.32±0.05	9.17±0.10	0.984±0.012
10	M1	Original TDR Design, Long traces	20.58±0.06	26.80±0.14	1.302±0.008
11	M1	Original TDR Design, Minimal traces	14.02±0.02	14.82±0.03	1.057±0.003
12	M1	Original TDR Design, Minimal traces, 0.5×Length, 2×Width	10.39±0.07	10.33±0.11	0.994±0.013

average interstrip capacitance as a function of strip number is presented. For most sectors, one can see a decrease in the interstrip capacitance near the center of the sector. This is due to the decreased signal trace length near the center of the sector. This is not the case for sector 11, as the traces that connect two adjacent strips are symmetrical,

and connect into opposite sides of the Panasonic connector. The measurements in sector 11 with the the grounding plate show a largely varying, antisymmetric trend in the interstrip capacitance, but the measurements without the plate show this effect of uniform interstrip capacitance across the sector. Sector 12 also exhibits higher interstrip capacitance for strips where the traces are longer, and decreases across the sector where the signal traces are shorter. For a detailed look at how the trace length and strip geometry/dimensions affect the interstrip capacitance across a sector, consider Fig. 7, which displays the interstrip capacitance as a function of strip number and a picture of the signal traces and readout strips for sector 5 (M1 module, original TDR design). Although the effect is not very large in this sector, the decreased trace length near the center of the sector is correlated with the decrease in interstrip capacitance.

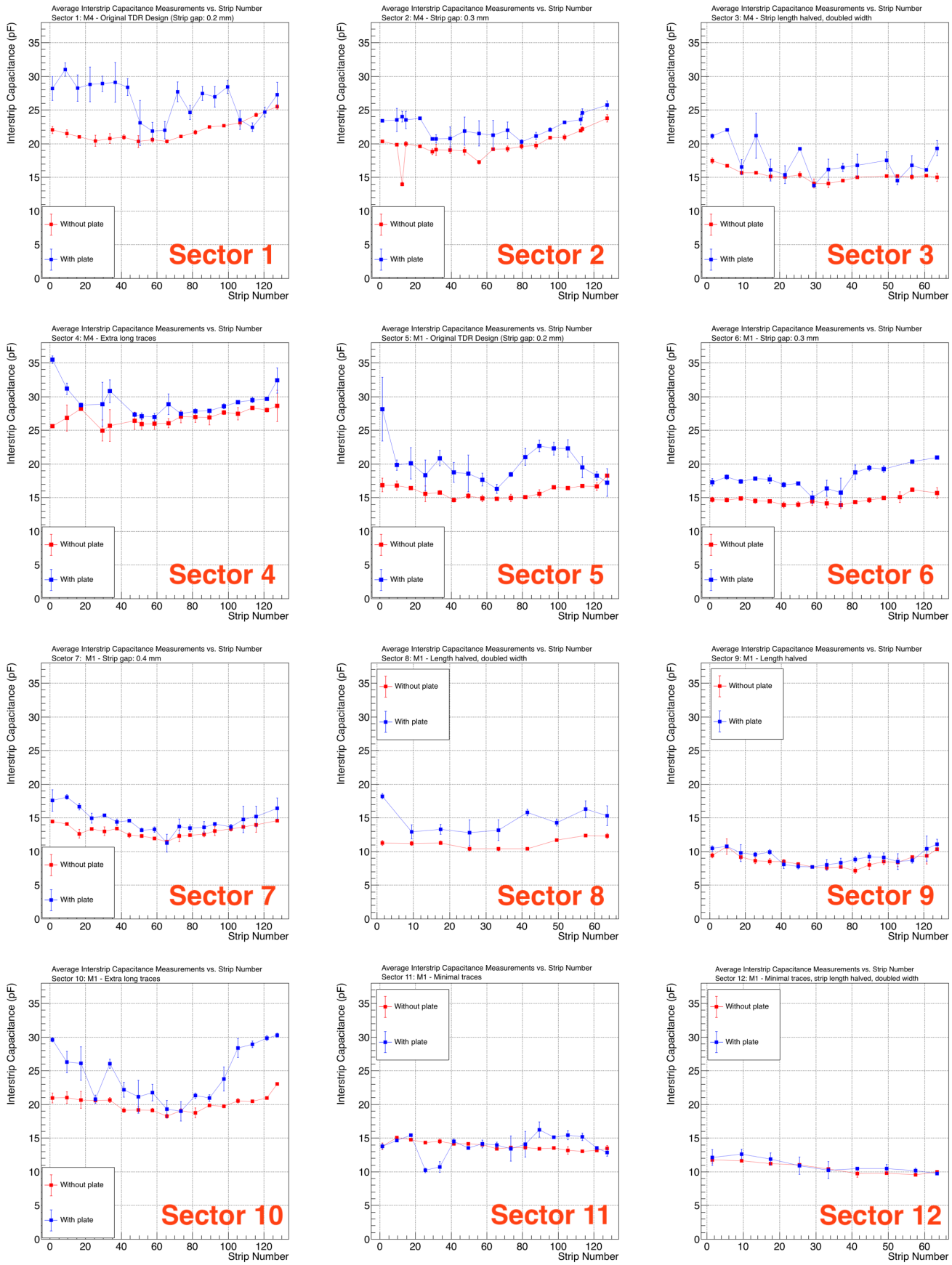

Figure 6: Average measured interstrip capacitances for all sectors, both with and without the copper-covered PCB, as a function of strip number.

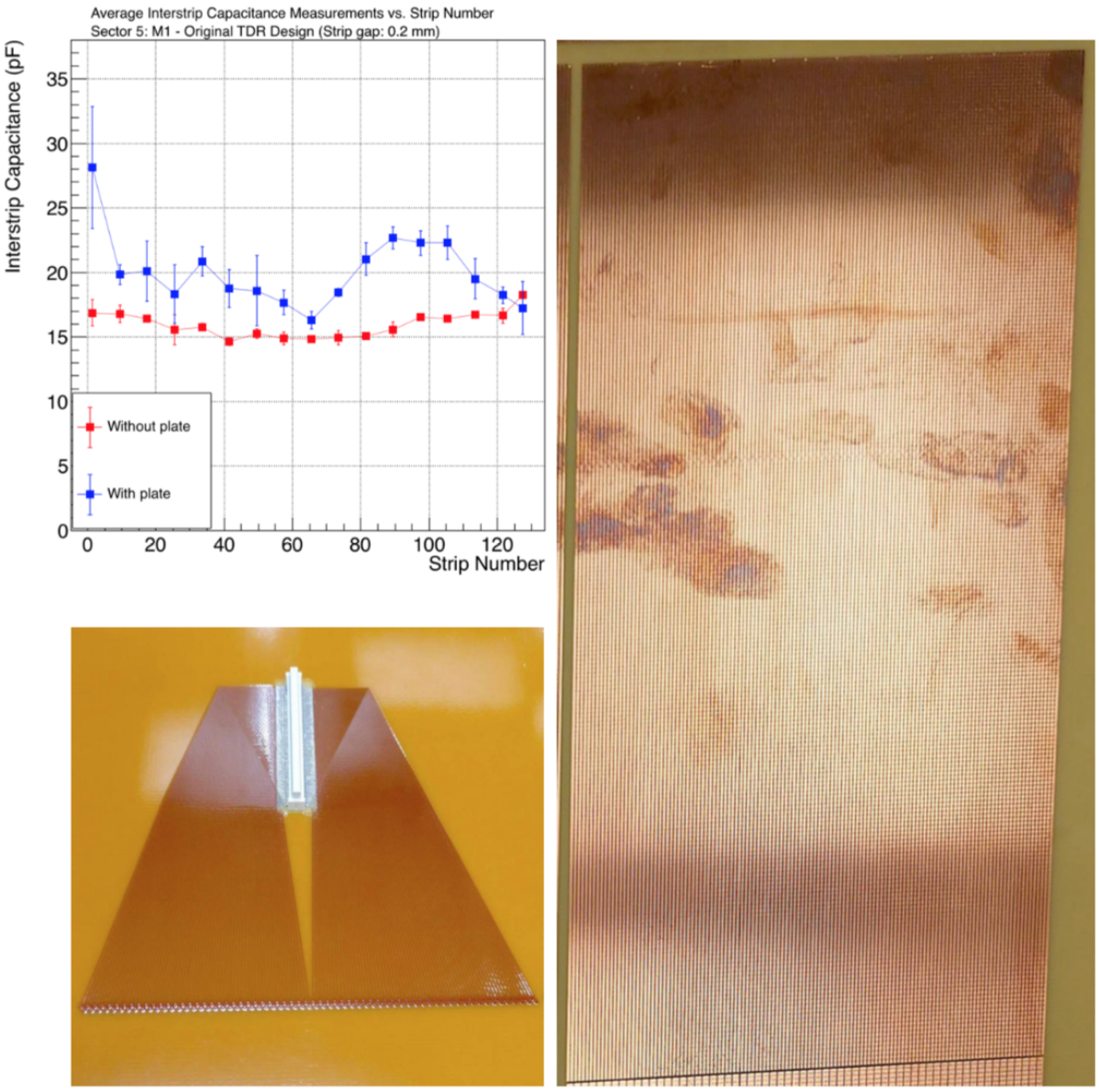

Figure 7: Average measured interstrip capacitances as a function of strip strip number for sector 5 and the associated signal trace (left) and strip (right) configuration. Due to the extended period of time the interstrip capacitance measurements took to complete, the copper readout strips became slightly oxidized while the board was uncovered in the cleanroom.

3 ENC Measurements

During a test campaign for GE1/1 readout electronics, which took place in November 2018, noise measurements were extracted from threshold scans for VFAT3 chips (S-curve measurements) at CERN for each of the twelve sectors on an identical ROB as the one used for the interstrip capacitance measurements presented here. This section will provide a brief presentation of the procedure of obtaining these measurements, and also their relationship to the interstrip capacitances of each of the twelve sectors.

3.1 Procedure

An S-curve is obtained by injecting a calibration pulse of fixed charge into one channel on the VFAT connected to a single sector. The channel is then read out for increasing values of the comparator voltage level to see if there is a positive or negative response from the comparator. This procedure is repeated for increasing levels of injected charge, and performed for all channels on the VFAT. A modified error function is fitted to the data. The resulting sigma is a measure of the of the equivalent noise charge (ENC). For more details on the procedure and the fitting algorithm, see [6].

Data were taken for all of the channels (strips) in each of the sectors on the ROB using this procedure. A histogram of the S-curve sigmas is plotted for varying levels of comparator voltage, and a Gaussian distribution is fitted to the points (results presented in [7]). The mean of the Gaussian function fit to these data points and its corresponding error are used as the figures of merit presented in the next section.

3.2 Results

The S-curve sigma measurements presented below were obtained from [7]. Due to a bad VFAT, S-curve measurements in sector 8 were not obtained. Below in Tab. 5, the S-curve sigma (ENC) and average measured interstrip capacitance for each sector are tabulated. These results are plotted against each other in Fig. 8. Note that the two outlying points in this dataset were excluded when fitting a linear model to the points. The outlying ENC values (sectors 3 and 4) were most likely due to noisy VFATs or improper grounding. Due to the lack of an extra chamber on which to fix the prototype ROB, these measurements were unable to be repeated.

Table 5: Average Measured Interstrip Capacitance w/o Plate and Measured ENC

Sector	Module	Parameters	Avg. Meas. Cap. (pF)	ENC (fC)
1	M4	Original TDR design (Strip Gap: 0.2 mm)	21.69 ± 0.05	0.56 ± 0.07
2	M4	Gap: 0.3 mm	19.98 ± 0.12	0.51 ± 0.08
3	M4	2xWidth, 0.5xLength	15.32 ± 0.03	0.93 ± 0.09
4	M4	Original TDR design, Long traces	27.87 ± 0.09	1.29 ± 0.02
5	M1	Original TDR design (Strip Gap: 0.2 mm)	16.27 ± 0.04	0.39 ± 0.05
6	M1	Gap: 0.3 mm	14.65 ± 0.07	0.30 ± 0.05
7	M1	Gap: 0.4 mm	13.17 ± 0.04	0.31 ± 0.03
8	M1	2×Width, 0.5×Length	11.82 ± 0.06	NA
9	M1	0.5×Length	9.32 ± 0.05	0.24
10	M1	Original TDR design, Long traces	20.07 ± 0.07	0.47 ± 0.05
11	M1	Original TDR design, Minimal traces	14.02 ± 0.02	0.38 ± 0.04
12	M1	Minimal traces, 0.5×Length, 2×Width	10.39 ± 0.07	0.36 ± 0.03

From the linear model, one can see that with increasing interstrip capacitance, the ENC increases, suggesting that the interstrip capacitance is positively correlated with ENC as expected. By removing the outliers, we obtain a more accurate fit to the data points. This shows that with every picofarad increase in interstrip capacitance, the ENC rises by about 0.022 fC ($\sim 131\, e^-$).

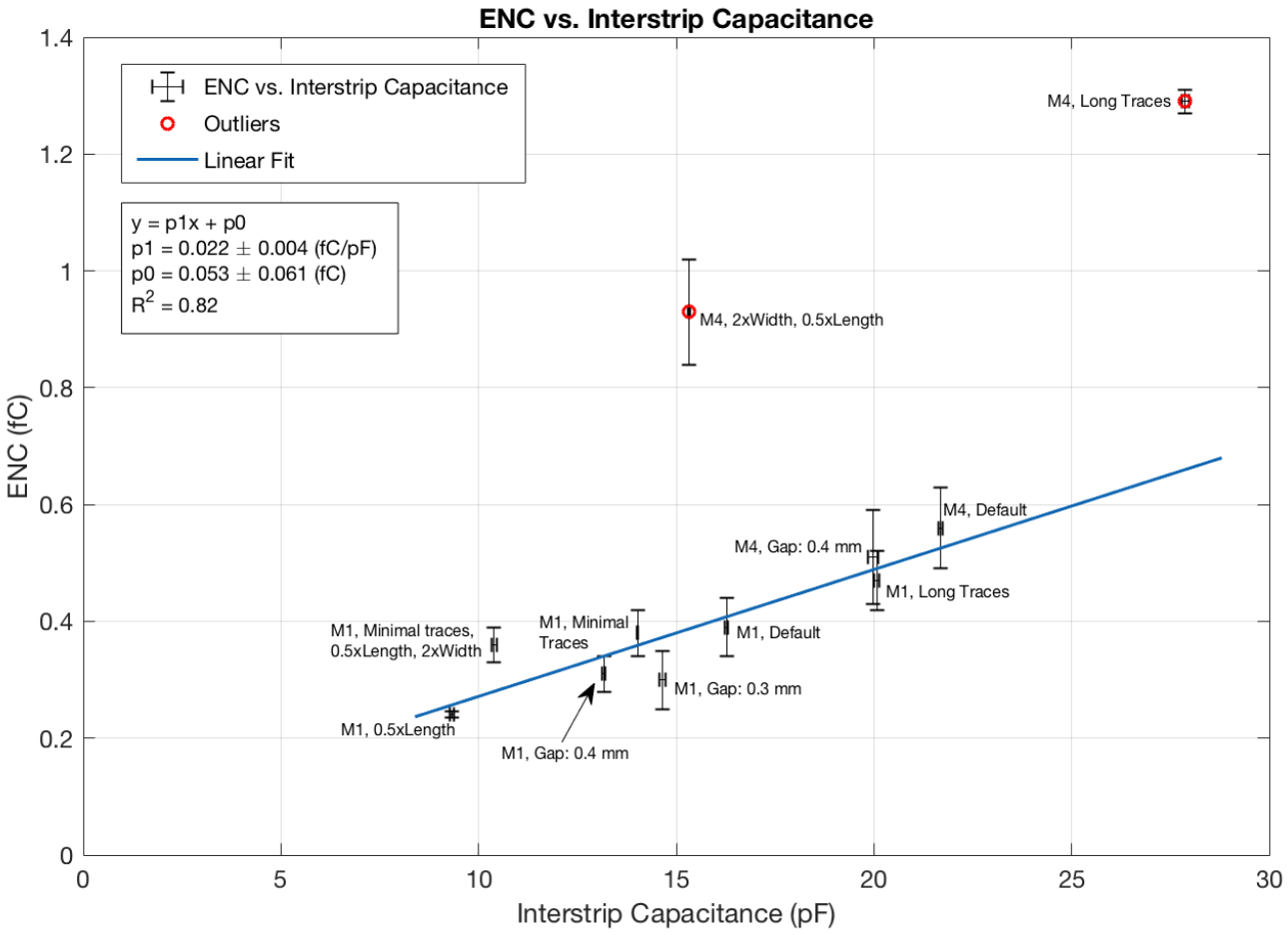

Figure 8: Plot of the measured ENC versus the measured interstrip capacitance with linear fit. Note that the data point for sector 8 is not displayed.

4 Summary and Conclusion

This note presents the approximate analytical calculations and the measured interstrip capacitances for twelve different strip geometries and dimensions that are currently under consideration for the M1 and M4 modules of the GE2/1 detector, as well as the relationship between the ENC and the interstrip capacitance. The strip dimensions that result in the lowest measured interstrip capacitance have doubled strip width and halved strip length in the M4 module ($C = 15.32 \pm 0.03$ pF), which is a 29% reduction in interstrip capacitance compared to the original TDR design, and for halved strip length in the M1 module ($C = 9.32 \pm 0.05$ pF), which is a 43% reduction in interstrip capacitance. An important conclusion drawn from the measurements of the interstrip capacitance is the effect the traces have on the capacitance; with longer trace lengths, the interstrip capacitance increases by about 30% in the M4 module and by about 23% in the M1 module. We have also seen, on average, a 15% increase in the interstrip capacitance with the addition of the copper-covered PCB which was used to simulate the capacitance contribution from the bottom of the third GEM foil. Increasing the width of the gaps between strips only produces a minor reduction in interstrip capacitance. The M1 module configuration with strip length halved also resulted in the lowest ENC at 0.24 fC (the ENC for the M4 module with the lowest interstrip capacitance was an outlier at 0.93 ± 0.09 fC). The results of comparing the ENC with the measured interstrip capacitance suggest that the noise in the detector is linearly correlated with the interstrip capacitance. As such, by minimizing the interstrip capacitance, the ENC from the ROB can be minimized, which will consequently improve the S/N ratio.

The hypothesis that prompted these studies was that reducing the strip lengths while increasing the strip widths proportionally should lead to a reduction of interstrip capacitances and noise due to the planar geometry even though the strip areas stay fixed in this modification. We conclude from our observations that this hypothesis is confirmed by both analytical calculations and direct measurements.

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