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Electronics integration for the GE2/1 and ME0 GEM detector systems for the CMS phase-2 muon system upgrade

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Abstract: The Large Hadron Collider is currently undergoing its High Luminosity upgrade, which is set to increase the instantaneous luminosity by about a factor of five. Consequently, the Compact Muon Solenoid experiment is upgrading its muon spectrometer to cope with the increased muon flux in the forward region. The GE2/1 triple-gas electron multiplier detector, which has recently entered the mass production phase, and the ME0 triple-GEM detector system, which is in the late prototyping phase, are undergoing electronics integration. These proceedings briefly discuss the frontend electronics for the GE2/1 and ME0 detector systems, the electronics integration testing process, and the future plans for the frontend electronics of these two detector systems by the CMS GEM collaboration.

Keywords: Front-end electronics for detector readout; Micropattern gaseous detectors (MSGC, GEM, THGEM, RETHGEM, MHSP, MICROPIC, MICROMEGAS, InGrid, etc.)

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Contents

1 Introduction

With the projected five-fold increase in instantaneous luminosity resulting from the High Luminosity upgrade of the Large Hadron Collider, the Compact Muon Solenoid (CMS) experiment is currently upgrading its muon spectrometer [1]. Two triple-Gas Electron Multiplier (GEM) detector systems — the GE2/1, currently in the early mass-production phase, and the ME0, currently in the prototyping phase — are undergoing frontend electronics integration. These proceedings discuss the current status of the electronics integration effort on full-size GE2/1 and ME0 chamber prototypes by the CMS GEM collaboration and the future prospects for the frontend electronics readout systems.

2 The GE2/1 and ME0 detector systems

The GE2/1 and ME0 are modular triple-GEM detector systems. Each GE2/1 chamber consists of four modules, namely the M5–M8 modules for the front GE2/1 chamber, and the M1–M4 modules for the back chamber (figure 1 (left)). When installed in the CMS experiment, a front and a back chamber will be mounted back-to-back, in front of the ME2/1 cathode strip chamber in the second muon station, covering the pseudorapidity range $1.62 < |\eta| < 2.43$. The ME0 detector system consists of six individual modules (see figure 2 (left)) stacked upon one another. These "stacks" will be inserted in the endcap nose behind the high granularity calorimeter, increasing coverage of the muon spectrometer between $2.0 < |\eta| < 2.8$.

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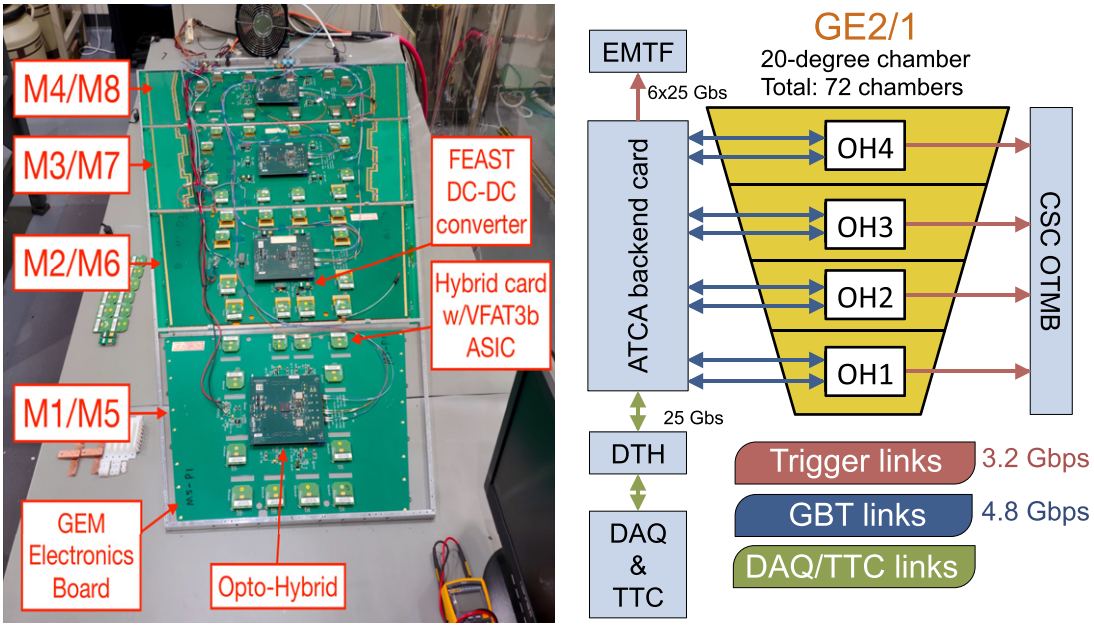

Figure 1. Full GE2/1 front chamber prototype with modules and frontend electronics indicated (left) and block diagram of the GE2/1 electronics with frontend Opto-Hybrid (OH) boards, backend Advanced Telecommunications Computing Architecture (ATCA) boards, and the connections from the backend ATCA board with the data acquisition (DAQ) and TTC Hub (DTH), the DAQ and timing, trigger and control (TTC) systems, the endcap muon track finder (EMTF), and the optical trigger motherboard (OTMB) of the Cathode Strip Chamber (CSC) system (right).

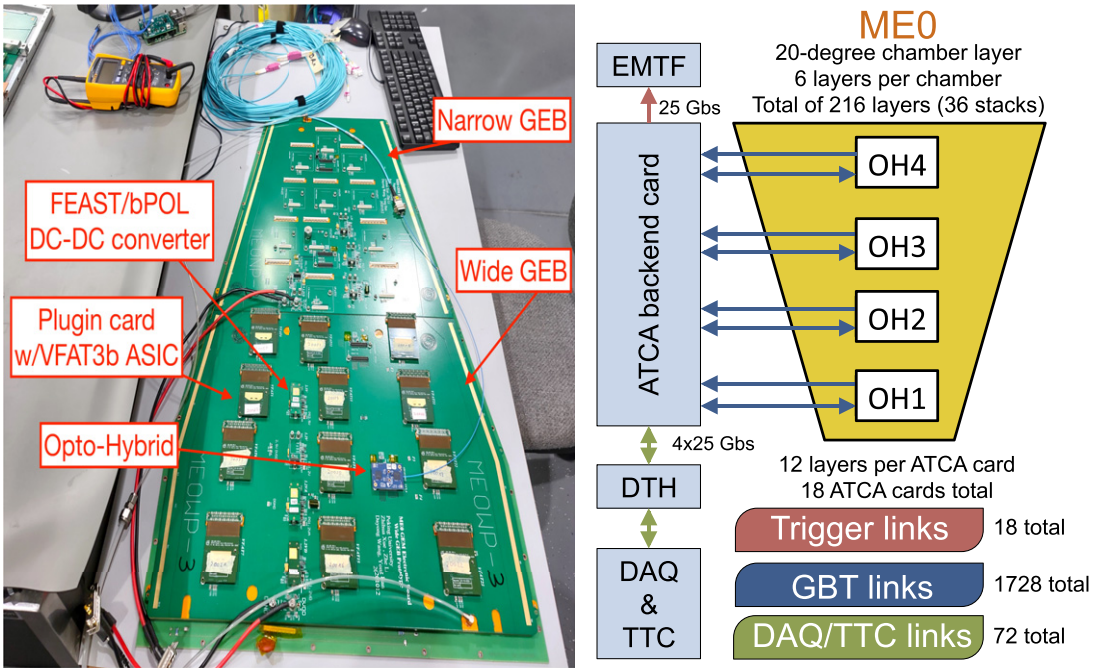

Figure 2. An ME0 prototype module with frontend electronics indicated (left) and block diagram of the frontend/backend electronics for the ME0 (right).

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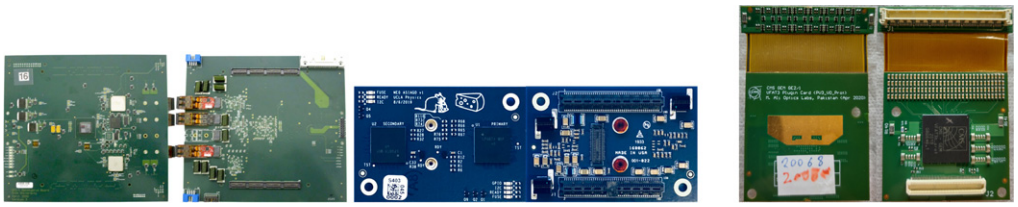
3 Frontend electronics for the GE2/1 and ME0

Both the GE2/1 and ME0 detectors share similar frontend electronics; see block diagrams for the GE2/1 and ME0 in figures 1 and 2 (right), respectively. For example, each GE2/1 module or ME0 layer will have a GEM electronics board (GEB), which is responsible for routing the signals from the readout (RO) application specific integrated circuits (ASICs) to the Opto-Hybrid (OH). Pictures of a full GE2/1 chamber and an ME0 module with their electronic components indicated are displayed in figures 1 and 2 (left), respectively. The GEB is fixed to the detector readout board that the inputs of the frontend readout ASICs are plugged into. The OH is responsible for communication between the frontend and backend, transmitting both data acquisition (DAQ) and trigger data via the Versatile TransReceiver (VTRx) and Versatile Twin Transmitter (VTTx) [2] on the GE2/1 OH, and the VTRx+ [3] on the ME0 OH. The GE2/1 OH [4] (figure 3(a)) features a Xilinx Artix-7 field programmable gate array (FPGA), which interfaces with two gigabit transceiver (GBT) ASICs that communicate with the frontend RO chips, and the GBT-Slow Control Adapter ASIC for slow control commands. Since the ME0 will operate in a radiation environment where the expected hit rate will reach up to ~150 kHz/cm^2, the ME0 OH [5] (see figure 3(b)) features two low-power GBT (LpGBT) chips and does not use an FPGA. The frontend RO ASICs are the packaged Very Forward ATLAS and TOTEM 3b (VFAT3b) chips mounted on a plug-in card [6] (figure 3(c)). One GE2/1 GEB is operated with one OH, which communicates with 12 VFATs, while one ME0 GEB (two GEBs per chamber) contains two OHs, each of which communicates with six VFATs a piece. Low voltage for the GE2/1 is distributed by FEASTMP_CLP DC-DC converters [7], while the ME0 will be powered by bPOL12V DC-DC converters [8].



(a) GE2/1 OH front (left) and back (right) [4].

(b) ME0 OH front (left) and back (right) [5].

(c) The front (left) and back (right) of the plugin card with VFAT3b ASIC [6].

Figure 3. Photos of the core frontend electronics for the GE2/1 and ME0 detector systems.

4 Frontend electronics integration testing

Frontend electronics integration for the GE2/1 and ME0 detector systems consist of several procedures and tests to establish communication, calibrate, and determine the noise in the system. For both detectors, the integration pipeline is identical, although there are some exceptions; (e.g., the ME0 OH does not have an FPGA, thus FPGA programming is skipped during the second step of the pipeline). See table 1 for a comprehensive list and explanation of the integration procedures.

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Table 1. Frontend electronics testing procedure.

Step	Procedure
0	Test the voltages produced by the DC-DC converters
1	Establish connectivity [check (Lp)GBT communication, check trigger links, program FPGA (GE2/1), GBT phase scans, check VFAT synchronization]
2	Retrieve VFAT calibration data from the database and program nominal register values
3	Calibrate VFATs by performing digital-to-analog converter scans to characterize and determine nominal values of programmable registers
4	Equivalent noise charge measurement for DAQ electronic links
5	S-bit noise measurement for trigger eLinks

Connectivity testing begins with first establishing communication with the OH, checking the trigger links, (programming the FPGA for GE2/1), and scanning the clock phases of the (Lp)GBTs to synchronize the VFATs to a common clock. Next, calibration data (internal current/voltage biases) are retrieved from the CMS GEM database, which are subsequently programmed into the VFATs. Characterization scans for each of the programmable digital-to-analog converters (DACs) on each VFAT are performed by scanning a range of register values and reading the output current/voltage with the internal analog-to-digital converter (ADC) of the VFAT. Optimal DAC values are determined from the resulting curves.

Equivalent noise charge (ENC) measurements (colloquially referred to as "S-curves" due to their shape) are then taken for the DAQ electronic links (eLinks) by injecting increasing amounts of charge into each channel and recording the comparator response, and then fitting a modified error function (equation (4.1)) to the data:

$$f(q) = A \cdot \mathrm{erf}\left(\frac{\max(p,q) - \mu}{\sigma\sqrt{2}}\right) + A \tag{4.1}$$

where q is the magnitude of injected charge, $A = n/2$, where n is the number of injected charges, p is the pedestal (recorded comparator responses with no injected charge), μ is the comparator threshold, and σ is the ENC derived from the fit. The criterion for a successful ENC measurement requires the average ENC of all channels to be 0.25 fC or less for all VFATs. Figure 4 (left) shows S-curves and their fit parameters for a few channels on one VFAT and figure 5 (left) shows S-curves for all 128 channels. From the ENC extracted from the fit in figure 4 (left), these three channels do not pass the required noise value. As displayed in figure 4 (right), we see the average ENC value for all channels on each of the six VFATs are about 0.4 fC, and all VFATs fail to meet the required noise threshold. In this case, the grounding of the electronic components on the ME0 layer and the mechanical frame are refined until all plugin cards reach acceptable noise levels. In the event that this fails, any plugin card that does not meet the noise requirement will be replaced and the entire frontend electronics testing procedure will be repeated. For production detectors, no dead VFAT channels are allowed. VFATs that have one or two dead channels are reserved for emergency use, while VFATs with more than two dead channels are completely rejected.

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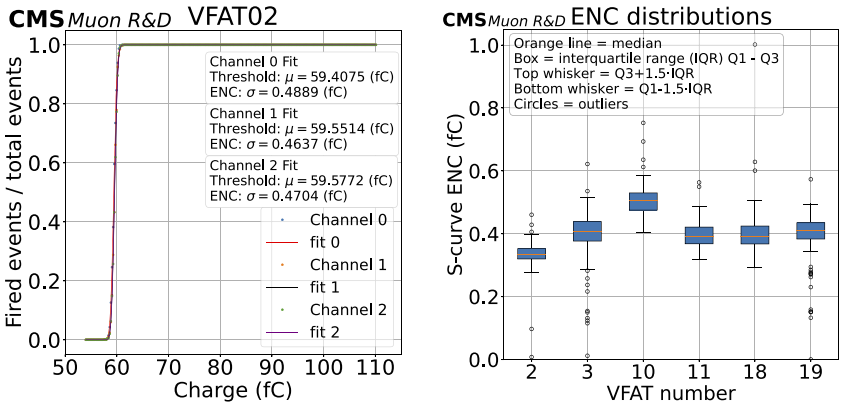

Figure 4. S-curves for three channels with fit data (left). S-curve sigma (ENC) distributions for all 128 channels for six VFATs on an ME0 GEB (right). Note that one outlier point for VFAT18 is not displayed.

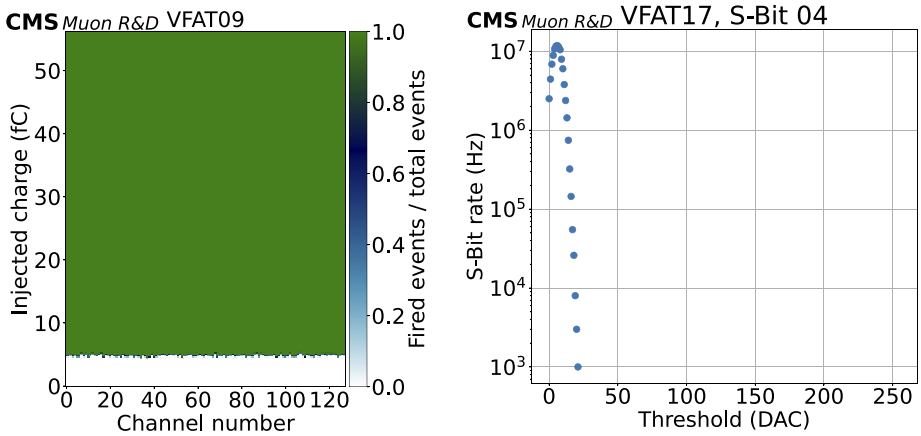

Figure 5. S-curves for all channels (left) and trigger S-bit noise rate measurement (right) for a single S-bit on one VFAT on an ME0 detector.

The last step is the noise measurement for the trigger eLinks. For triggering purposes, the RO strips (connected to the VFATs) are paired, resulting in 64 strip groups, or "S-bits". For GE2/1, the RO strips in the vertically adjacent or neighboring eta sectors are paired (i.e., channel 1 from one VFAT is paired with channel 1 from another VFAT in the neighboring RO sector), while in ME0, horizontally adjacent strips in the same RO sector are paired together. When one (or both) of the two strips is (are) triggered, an S-bit is recorded. To determine the noise, the threshold is fixed, and one by one each S-bit is unmasked and counts are recorded. This is repeated for the entire DAC range of $[0, 255]$. The noise is thus determined by considering each individual S-bit (see an example in figure 5 (right)), and the cumulative sum and average of all S-bits for each VFAT. For a successful noise measurement of the trigger eLinks, the average noise at a threshold of 35 DAC units must be 10 kHz or less. Figure 5 (right), shows that for this single S-bit the noise at 35 DAC units is well below 1 kHz, thus meeting the acceptance criterion. Similar to the S-curve

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criterion, VFATs that have one or two dead S-bits are reserved for emergency use only, and VFATs with more than two dead S-bits are rejected.

5 Summary of GE2/1 and ME0 electronics integration status and plans

With the GE2/1 prototype electronics integration efforts at CERN, Rice University, Texas A & M, and Florida Tech coming to a close, mass production of GE2/1 GEM detectors has been initiated. All electronic components for GE2/1 are projected to be manufactured and tested by February of 2022, and full electronics integration with manufactured chambers expected to be complete by February of 2023. The ME0 electronics integration effort is ongoing, with component testing and electronics integration at CERN, UCLA, and Florida Tech. Recently, the second version pre-production OH was approved for manufacturing, and will begin production once the version 1 LpGBTs have been tested. The ME0 GEB is in its final prototyping stages, which will soon be reviewed for production. The collaboration is also currently testing an ATCA backend card with various FPGAs and optics, with a final design to be ready by early 2022. Manufacturing and testing of the ME0 on-chamber electronics is projected to be completed by November 2022, with all detector stacks to be installed in the new endcap nose by February 2026.

Acknowledgments

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