Undergraduate Research

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Abstract

While there were many tasks accomplished during this short summer semester, the main focus was testing the LV board which will be used in the GE2/1 stand. This testing was done for all 8 channels of the LV board which consumed a large portion of time due to the difficulties of the soldering process and other certain problems that were resolved. The results of the LV board test are described in this report along with a short section on THGEM measurements and preAmp testing.

1 Equipment

1. CAEN SY5527 Power Supply
2. A2519 50W LV Board
3. Variable Resistor 50Ω 50W 10% LUGS (AVT50-50-ND)

2 Low Voltage Board

The low voltage board was tested to ensure that it gives an accurate voltage when used in GE2/1. This test was done for all 8 channels in the A2519 50W LV board by measuring the monitored voltage and the sense wire voltage and comparing them to the set voltage. The following circuit was constructed and connected to the power supply and LV board for measuring

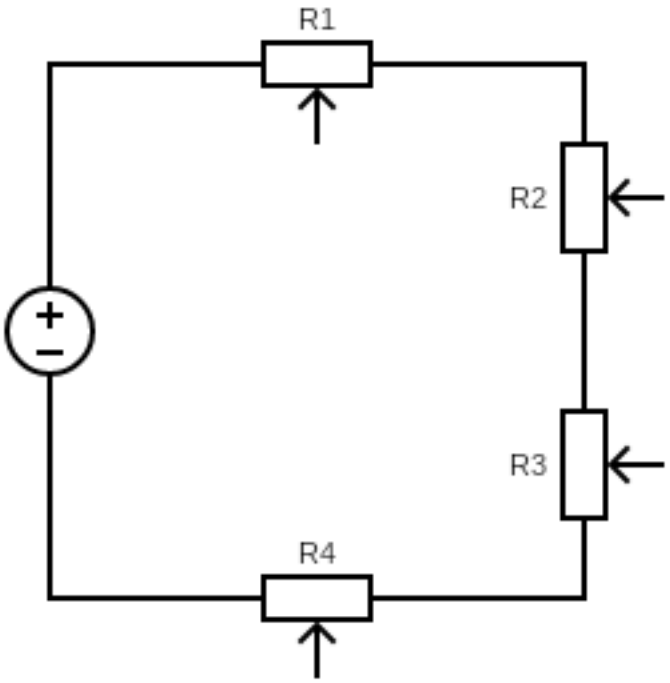

Figure 1: Four variable resistors in series

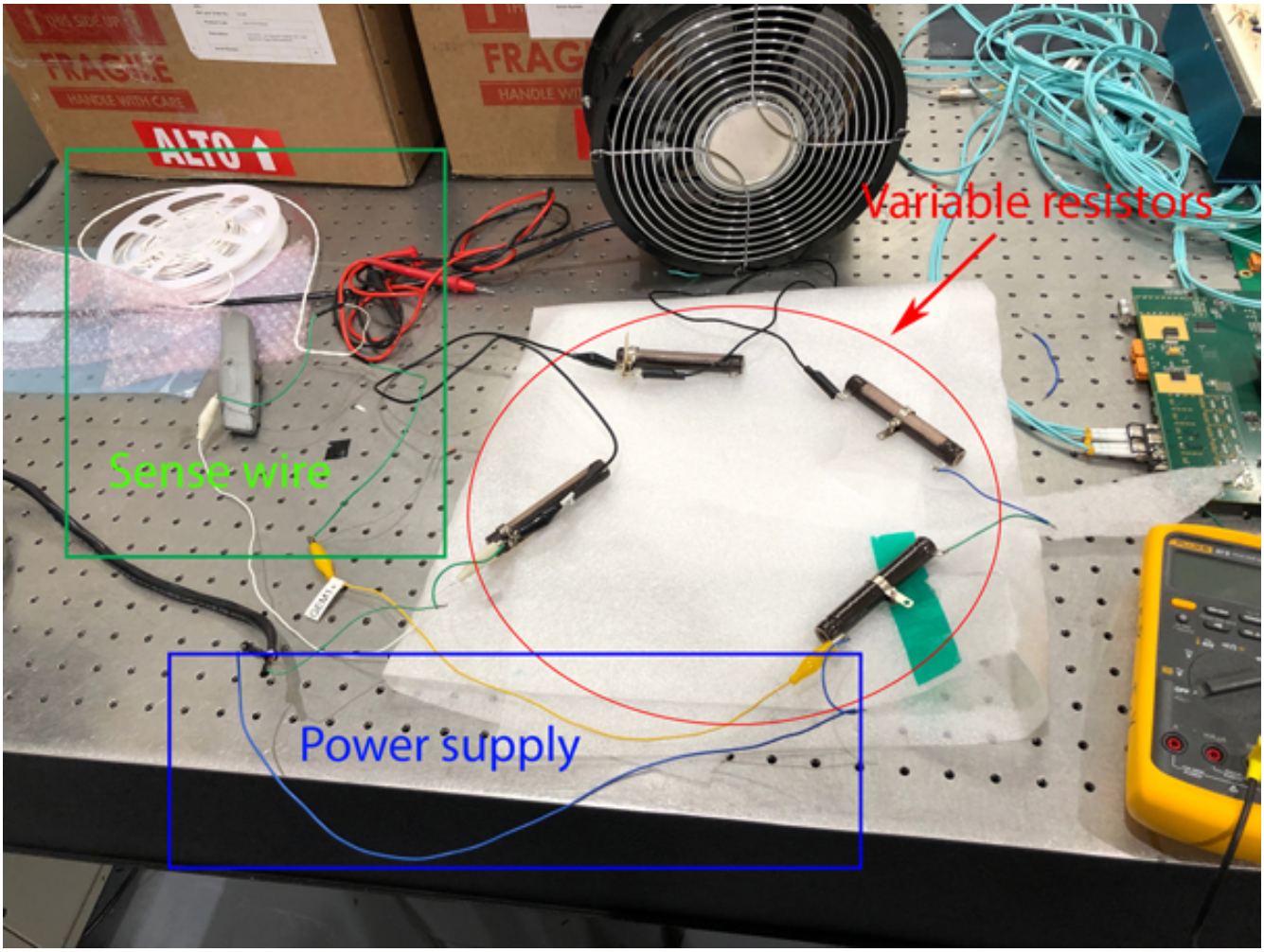

Figure 2: The circuit was initially connected through the breadboard but was then connected by wires due to inaccurate reading caused by the high current in the breadboard. It was then placed on an insulating surface due to metallic contact between the table and the resistors.

The circuit was constructed using four 50W variable resistors in order to dissipate more power and heat due to the high current. Data was recorded as the set voltage was varied from 5V to 14V. Each resistor was set to about 1 or 2 Ω such that the total resistance is 6 Ω. The monitored voltage, set voltage, and monitored current were recorded along with an extra measurement of voltage using the Multimeter and are shown in the tables below.

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error(V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5	5.265	4.999	0.027	0.937	0.95	1
6	6.002	6.322	6	0.032	1.124	0.949	1
7	7.002	7.377	7	0.037	1.312	0.949	1
8	8.001	8.425	8	0.042	1.5	0.95	1
9	9.002	9.481	9	0.047	1.688	0.949	1
10	10.004	10.537	10	0.052	1.877	0.949	1
11	11.008	11.592	11	0.057	2.064	0.95	1.001
12	12.006	12.644	12	0.062	2.251	0.95	1.001
13	12.997	13.69	13	0.067	2.438	0.949	1
14	13.996	14.747	14	0.072	2.626	0.949	1

Table 1: CH7

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5.002	5.27	5.005	0.027025	0.88	0.92	0.999
6	6.001	6.321	6.003	0.032015	1.105	0.949	1
7	7.001	7.373	7	0.037	1.291	0.95	1
8	8.001	8.425	8	0.042	1.476	0.95	1
9	8.997	9.474	9	0.047	1.661	0.95	1
10	10.005	10.537	10	0.052	1.894	0.95	1.001
11	10.999	11.583	11	0.057	2.034	0.95	1
12	12.002	12.638	12	0.062	2.221	0.95	1
13	13.009	13.695	13	0.067	2.408	0.95	1.001
14	14.005	14.749	14	0.072	2.594	0.95	1

Table 2: CH6

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5.001	5.257	4.999	0.026995	0.912	0.92	1
6	5.998	6.308	6	0.032	1.096	0.951	1
7	7	7.361	7	0.037	1.283	0.951	1
8	7.998	8.407	7.99	0.04195	1.467	0.951	1.001
9	8.999	9.464	9	0.047	1.653	0.951	1
10	10.003	10.519	10	0.052	1.837	0.951	1
11	11	11.57	10.99	0.05695	2.022	0.951	1.001
12	12.001	12.624	12	0.062	2.208	0.951	1
13	12.998	13.665	12.99	0.06695	2.39	0.951	1.001
14	14	14.724	13.99	0.07195	2.575	0.951	1.001

Table 3: CH5

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5.001	5.257	5.001	0.027005	0.903	0.92	1
6	6.001	6.308	6	0.032	1.087	0.951	1
7	7.001	7.359	7	0.037	1.268	0.951	1
8	7.999	8.407	8	0.042	1.454	0.951	1
9	8.999	9.459	9	0.047	1.638	0.951	1
10	10.003	10.516	10	0.052	1.822	0.951	1
11	10.998	11.549	10.99	0.05695	2.006	0.952	1.001
12	11.999	12.62	12	0.062	2.192	0.951	1
13	12.999	13.665	12.99	0.06695	2.376	0.951	1.001
14	13.997	14.715	13.99	0.07195	2.559	0.951	1.001

Table 4: CH4

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5.002	5.201	5.025	0.027125	0.918	0.92	0.995
6	6.004	6.242	6.028	0.03214	1.104	0.962	0.996
7	7.006	7.283	7.03	0.03715	1.29	0.962	0.997
8	8.001	8.318	8.04	0.0422	1.476	0.962	0.995
9	9.006	9.363	9.05	0.04725	1.664	0.962	0.995
10	10.004	10.4	10.05	0.05225	1.852	0.962	0.995
11	11.001	11.437	11.05	0.05725	2.038	0.962	0.996
12	12.002	12.478	12.06	0.0623	2.229	0.962	0.995
13	13	13.518	13.06	0.0673	2.415	0.962	0.995
14	14.002	14.558	14.07	0.07235	2.605	0.962	0.995

Table 5: CH3

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5.002	5.246	5.002	0.02701	0.867	0.92	1
6	6	6.295	6	0.032	1.044	0.953	1
7	6.994	7.34	7	0.037	1.22	0.953	0.999
8	7.998	8.392	8	0.042	1.398	0.953	1
9	8.998	9.442	8.99	0.04695	1.575	0.953	1.001
10	9.994	10.488	9.99	0.05195	1.752	0.953	1
11	11.001	11.542	10.99	0.05695	1.923	0.953	1.001
12	11.992	12.583	11.99	0.06195	2.09	0.953	1
13	13	13.639	12.99	0.06695	2.265	0.953	1.001
14	13.997	14.686	13.99	0.07195	2.441	0.953	1.001

Table 6: CH2

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	4.999	5.196	5.015	0.027075	0.932	0.92	0.997
6	5.999	6.234	6.02	0.0321	1.12	0.962	0.997
7	6.998	7.272	7.02	0.0371	1.308	0.962	0.997
8	7.994	8.309	8.02	0.0421	1.497	0.962	0.997
9	8.996	9.353	9.03	0.04715	1.685	0.962	0.996
10	9.994	10.387	10.03	0.05215	1.873	0.962	0.996
11	10.992	11.426	11.03	0.05715	2.063	0.962	0.997
12	11.991	12.465	12.03	0.06215	2.249	0.962	0.997
13	12.991	13.502	13.04	0.0672	2.437	0.962	0.996
14	13.988	14.544	14.04	0.0722	2.626	0.962	0.996

Table 7: CH1

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5.001	5.195	5.02	0.0271	0.917	0.92	0.996
6	6.001	6.234	6.024	0.03212	1.104	0.963	0.996
7	6.998	7.267	7.02	0.0371	1.288	0.963	0.997
8	7.999	8.309	8.03	0.04215	1.475	0.963	0.996
9	9.002	9.349	9.03	0.04715	1.661	0.963	0.997
10	10.002	10.388	10.04	0.0522	1.847	0.963	0.996
11	11.003	11.428	11.05	0.05725	2.034	0.963	0.996
12	12.006	12.467	12.05	0.06225	2.222	0.963	0.996
13	13	13.5	13.05	0.06725	2.41	0.963	0.996
14	13.998	14.543	14.05	0.07225		0.963	0.996

Table 8: CH0

I-V curves were plotted for both monitored and set voltage vs monitored current for all 8 channels. The graphs below show the data points that were measured along with a best fit line which is used to calculate the monitored resistance in the circuit.

CH7

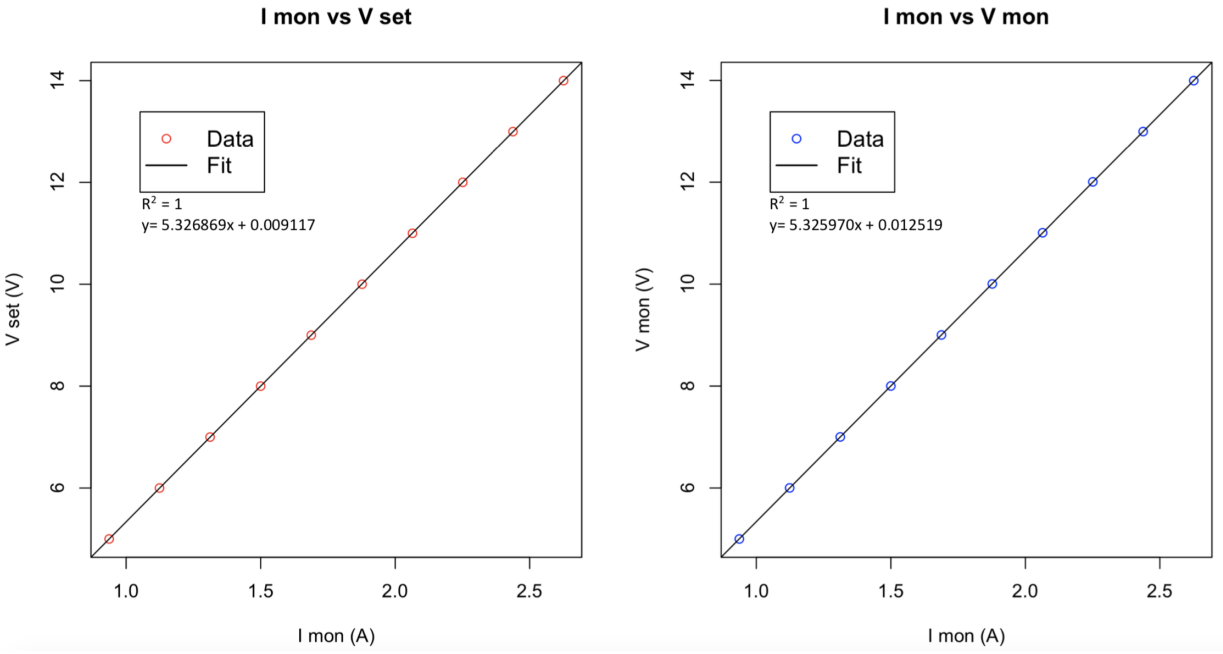

Figure 3: CH7

CH6

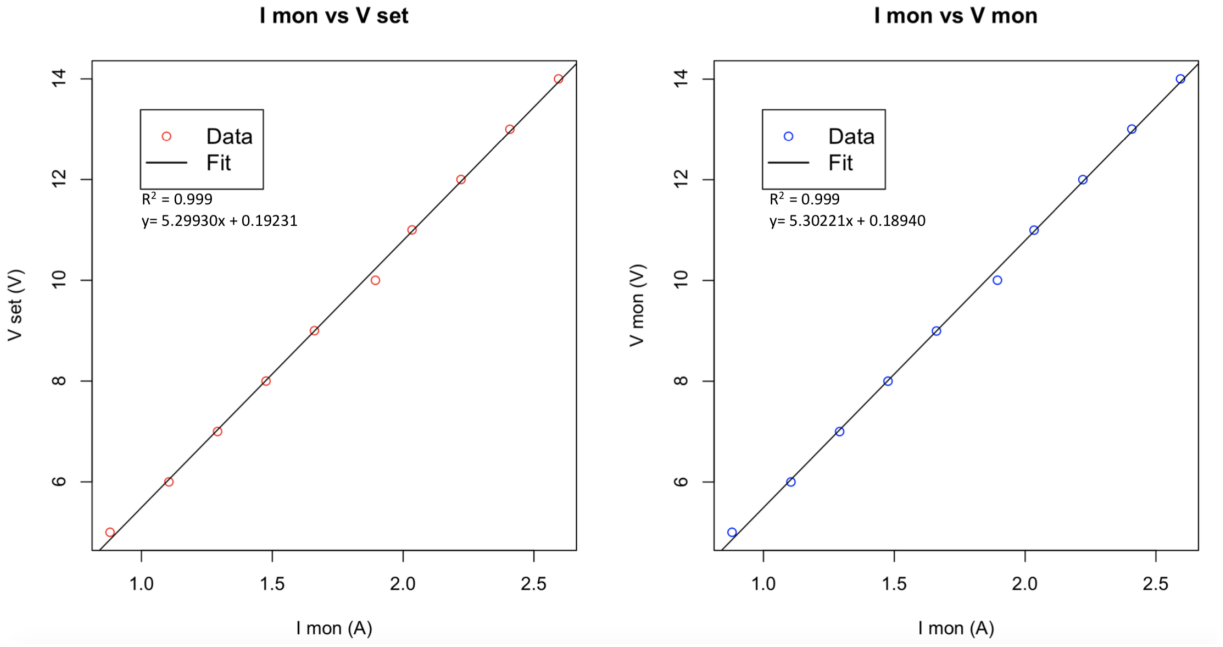

Figure 4: CH6

CH5

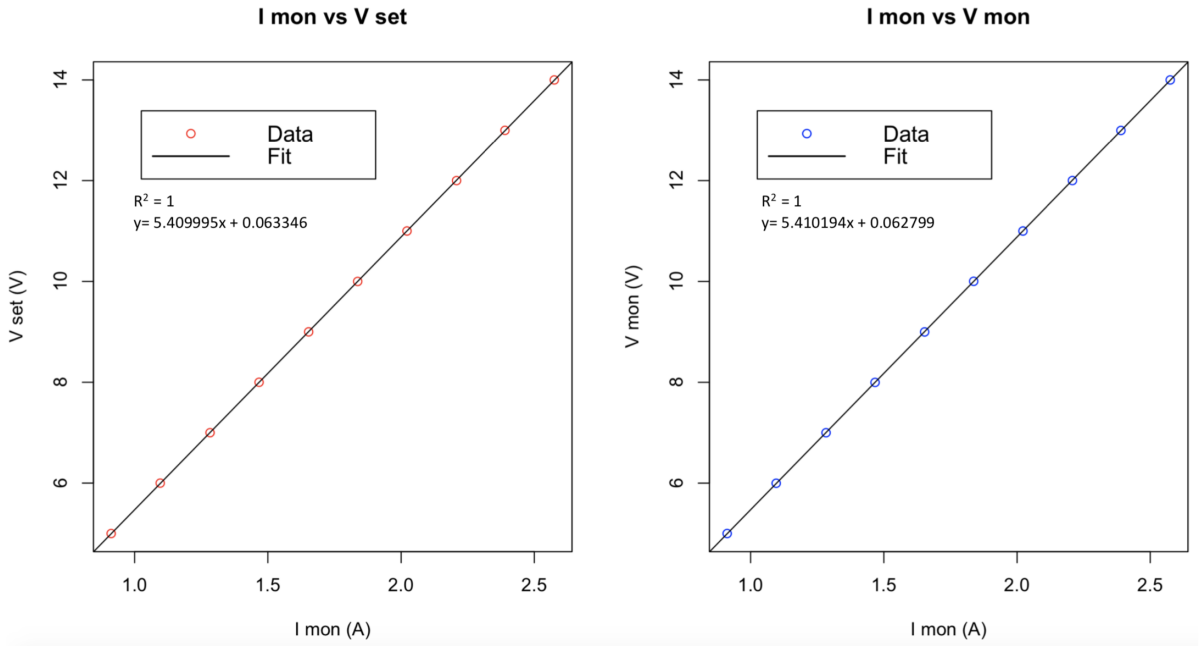

Figure 5: CH5

CH4

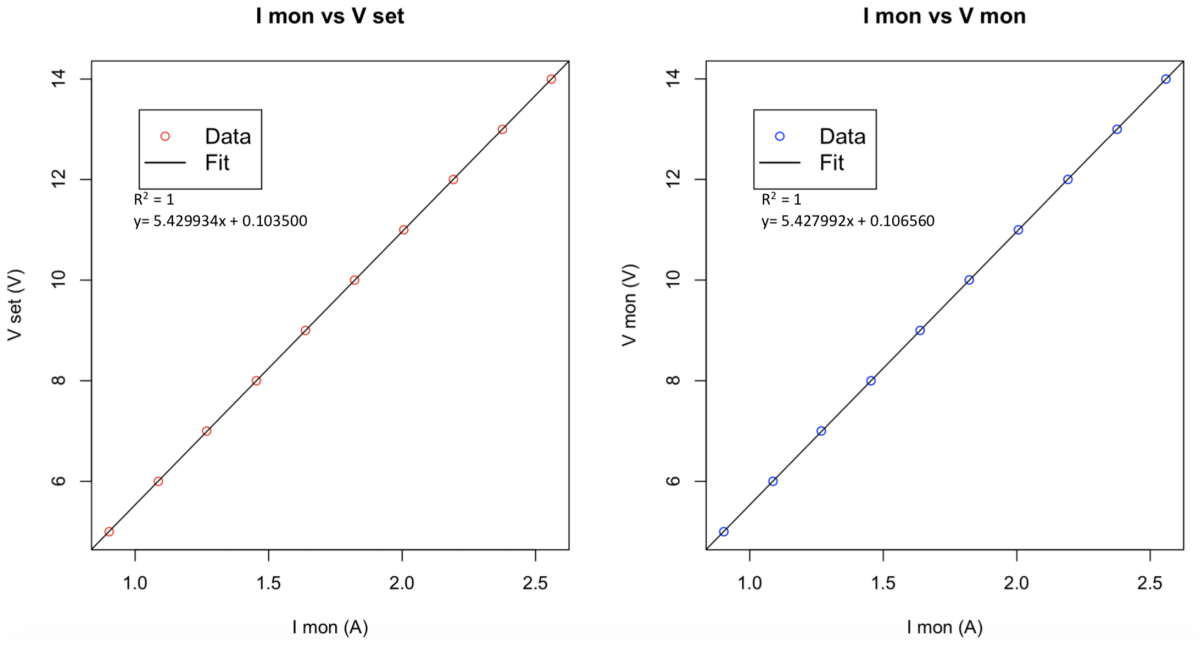

Figure 6: CH4

CH3

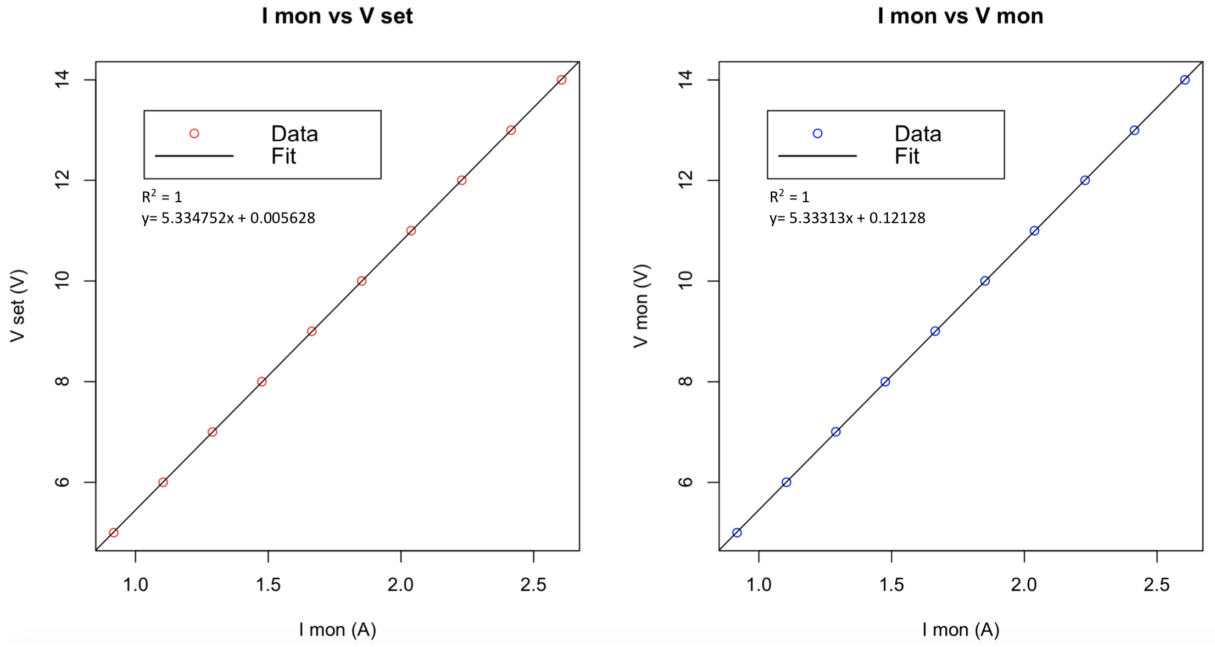

Figure 7: CH3

CH2

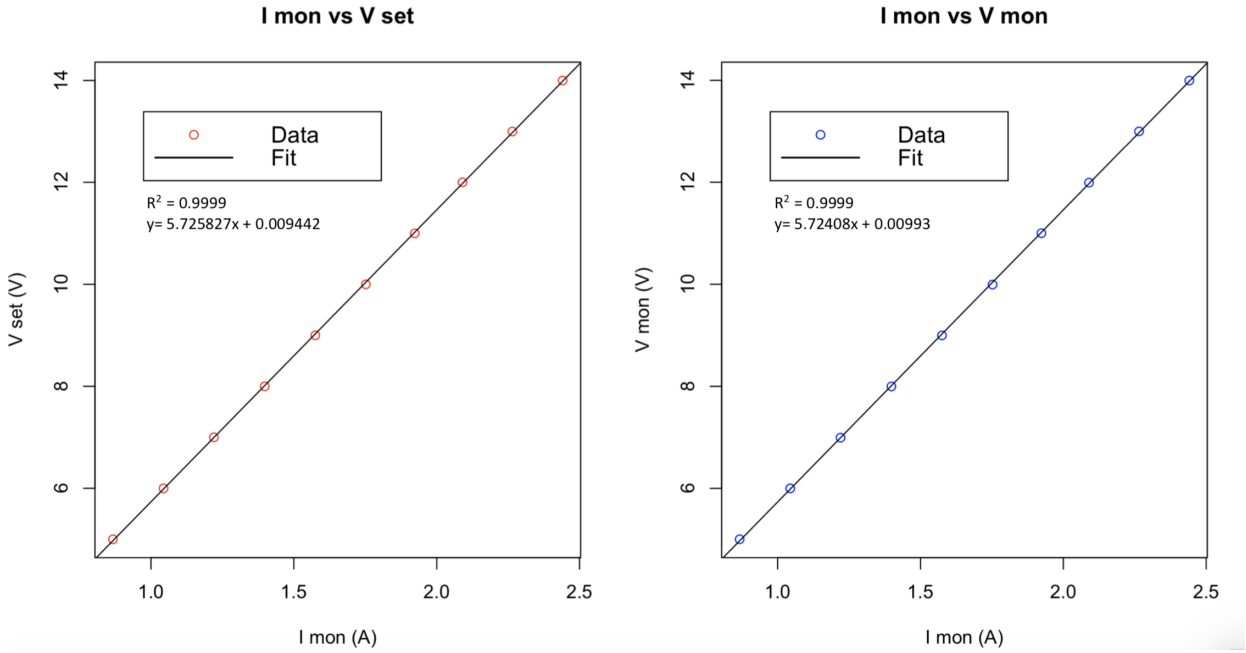

Figure 8: CH2

CH1

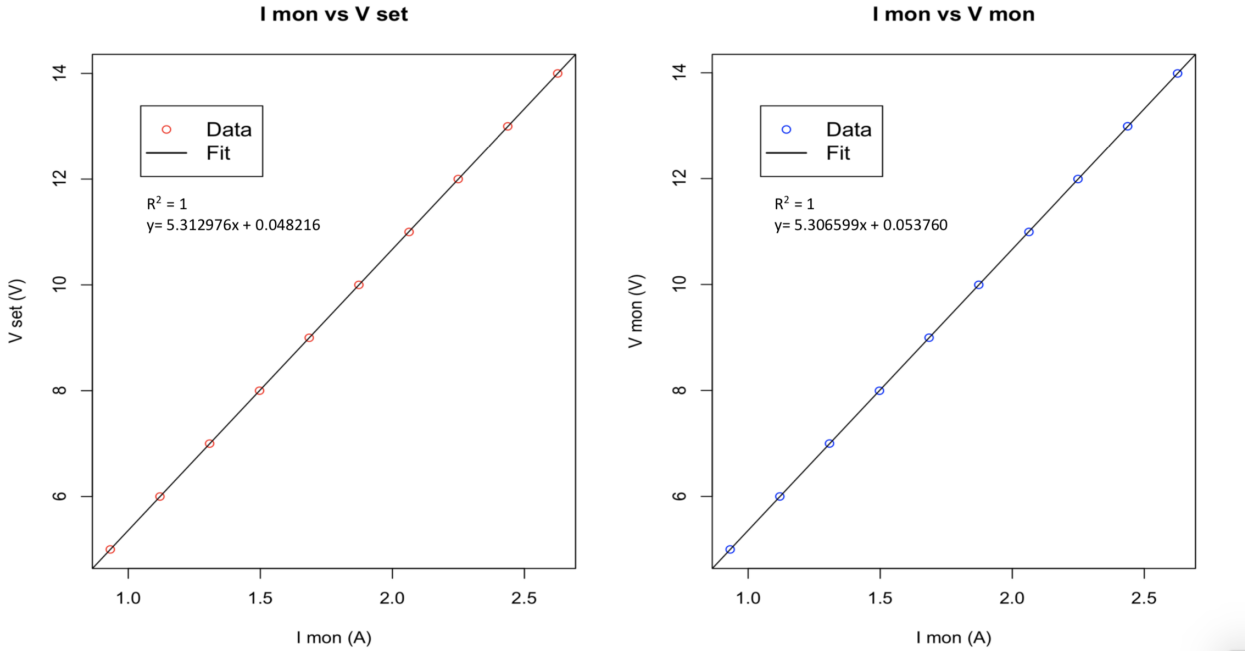

Figure 9: CH1

CH0

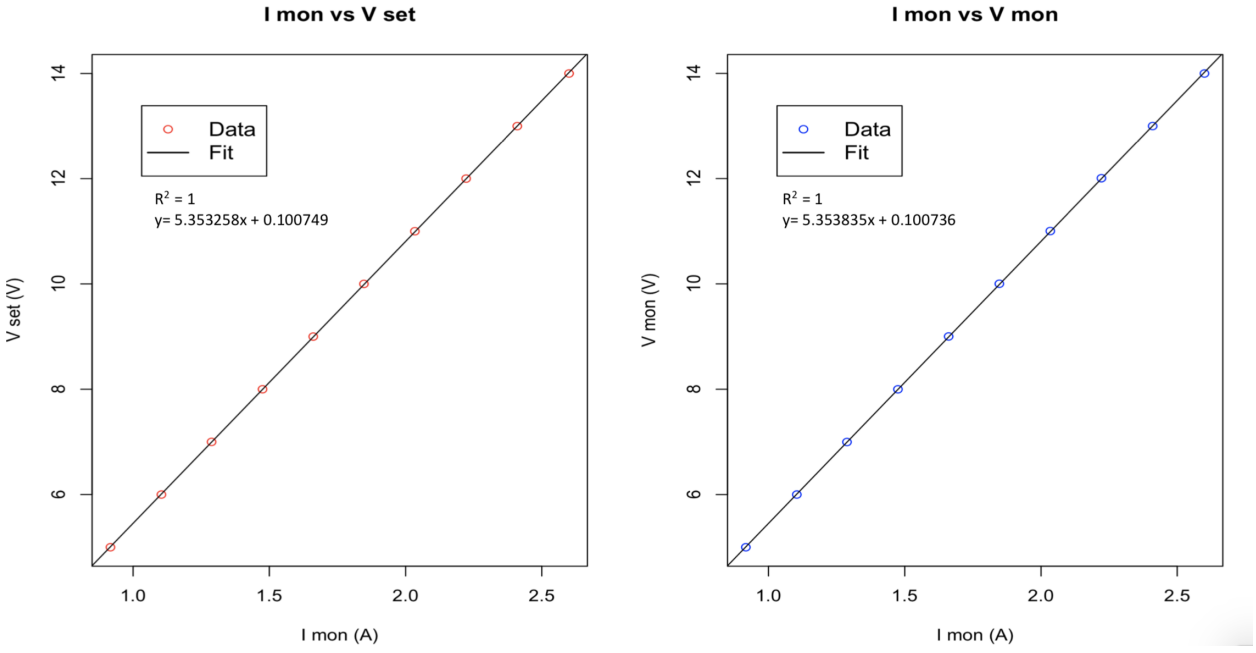

Figure 10: CH0

Although the resistance was set to 6Ω, due to the length of the sense wire, it was calculated to be lower from the I-V curves. The slope of I-V curves (resistance) for each channel is shown in the table below

CH	R (Vset)(Ω)	R (Vmon) (Ω)
0	5.353258	5.353835
1	5.312976	5.306599
2	5.725827	5.72408
3	5.334752	5.33313
4	5.429934	5.427992
5	5.409995	5.410194
6	5.29930	5.30221
7	5.326869	5.325970

Table 9: The resistance calculated for each channel using the I-V curves of both Vset and Vmon

A noticeable difference was observed between the monitored voltage and the sensed voltage due to the length of the sense wire. These voltages were plotted together against current to demonstrate how they vary as the current is increased.

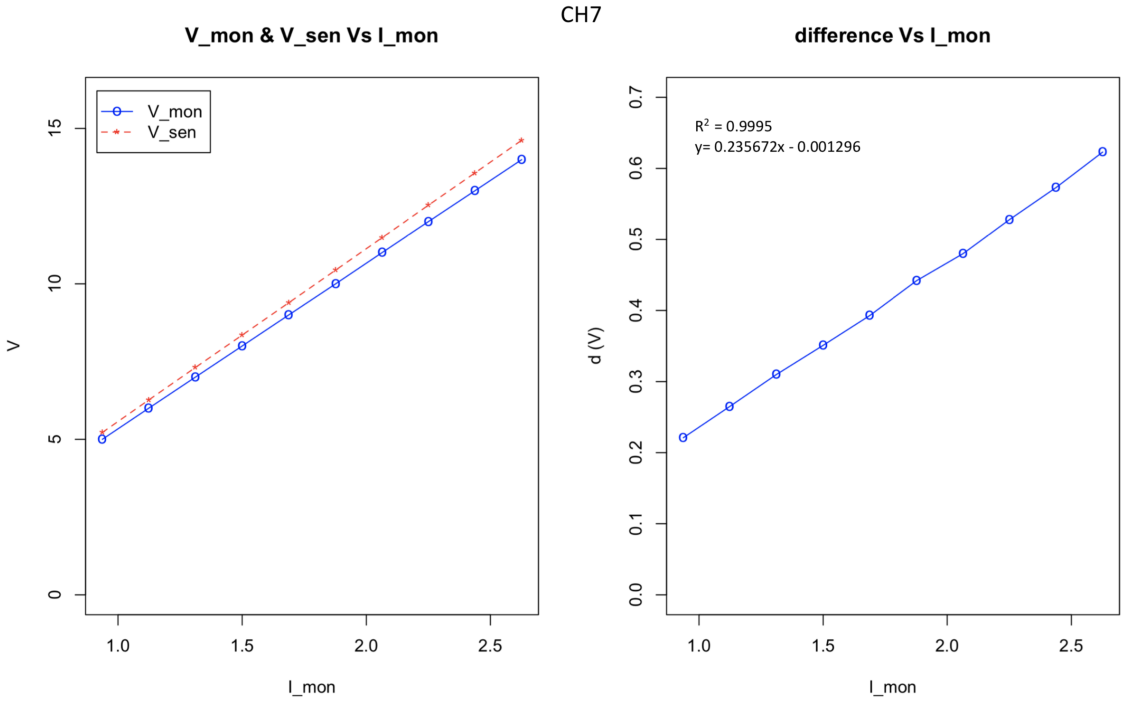

Figure 11: CH7

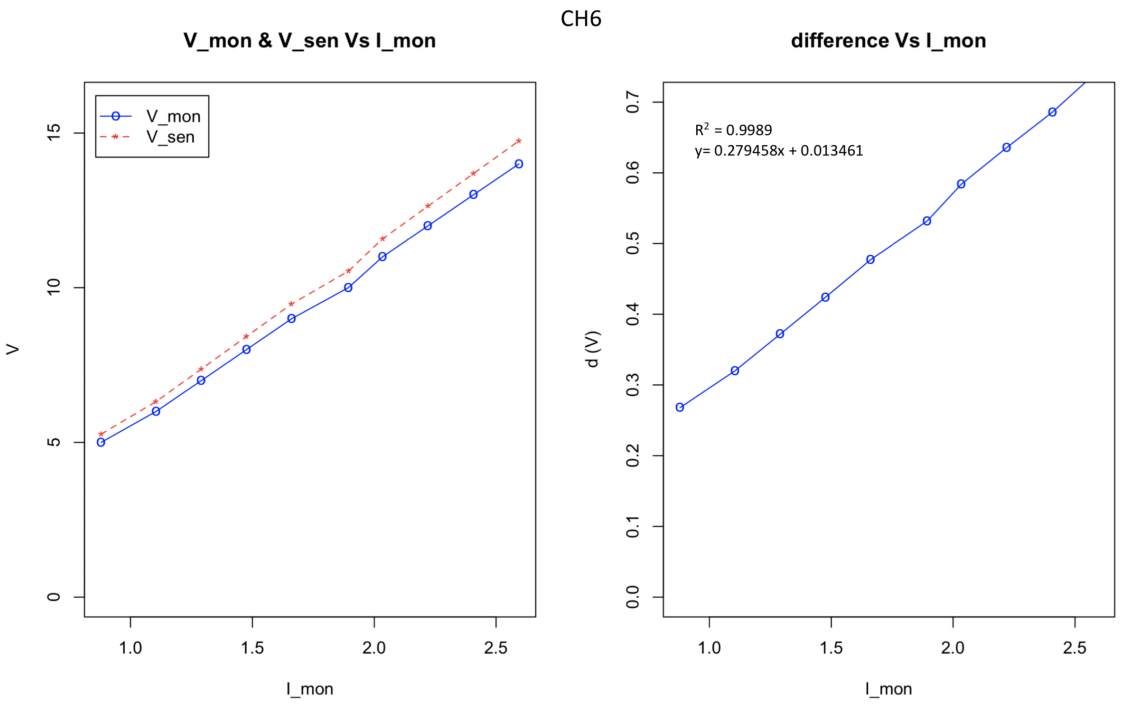

Figure 12: CH6

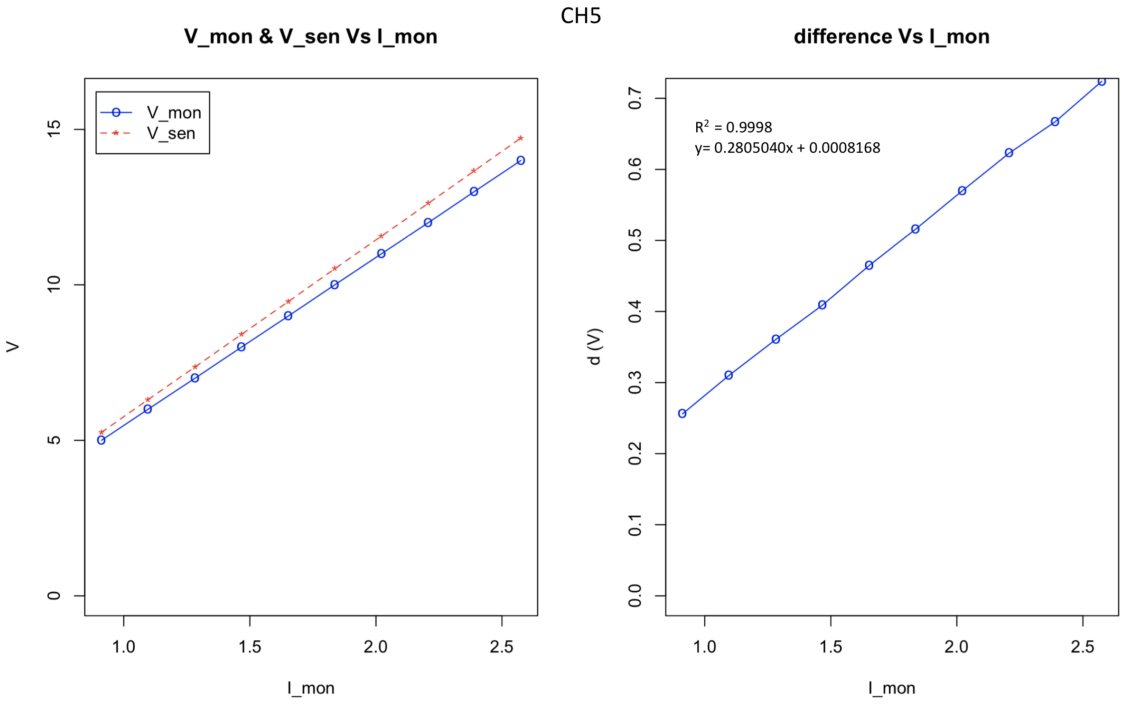

Figure 13: CH5

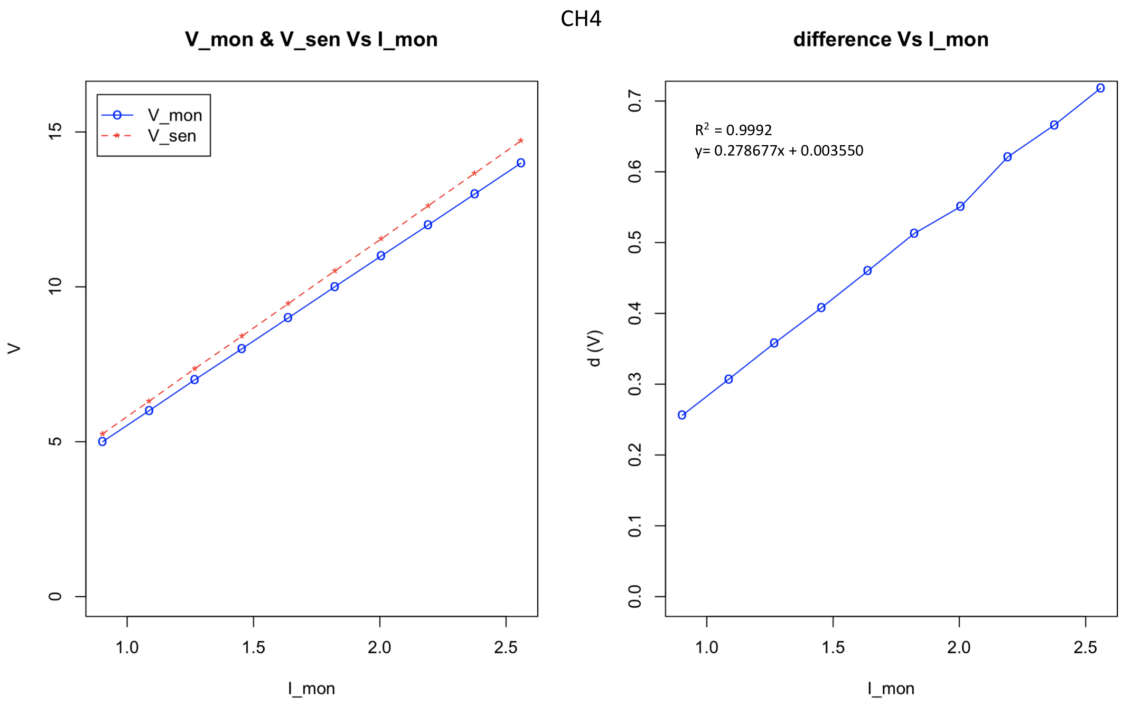

Figure 14: CH4

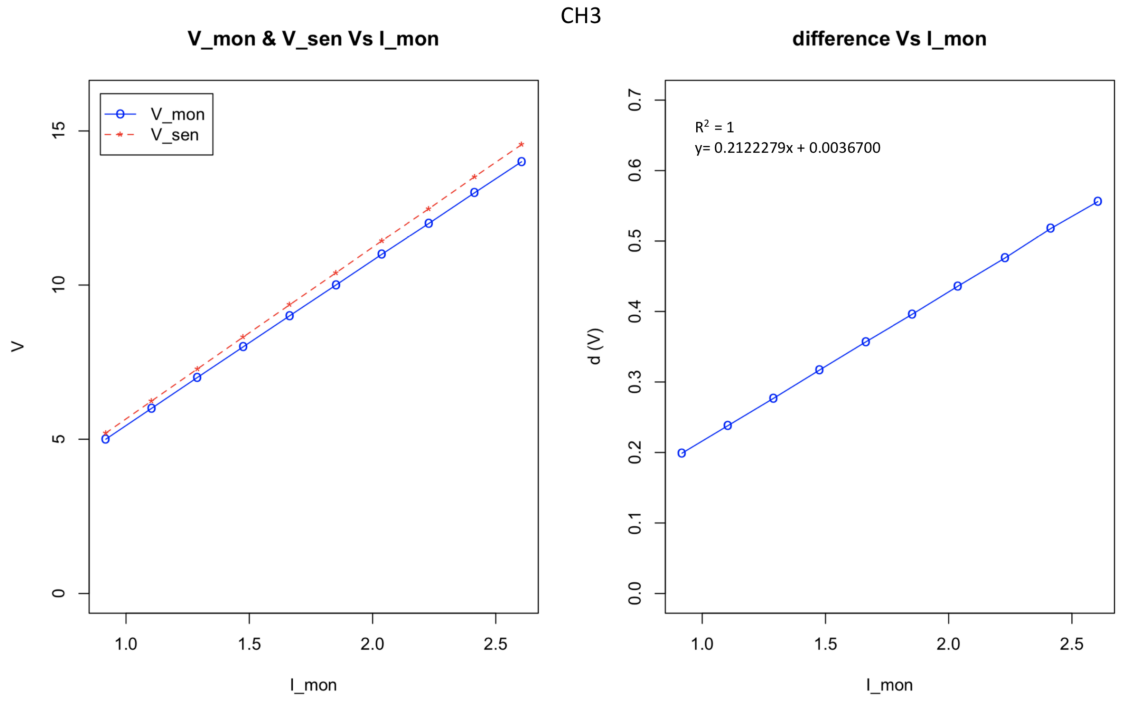

Figure 15: CH3

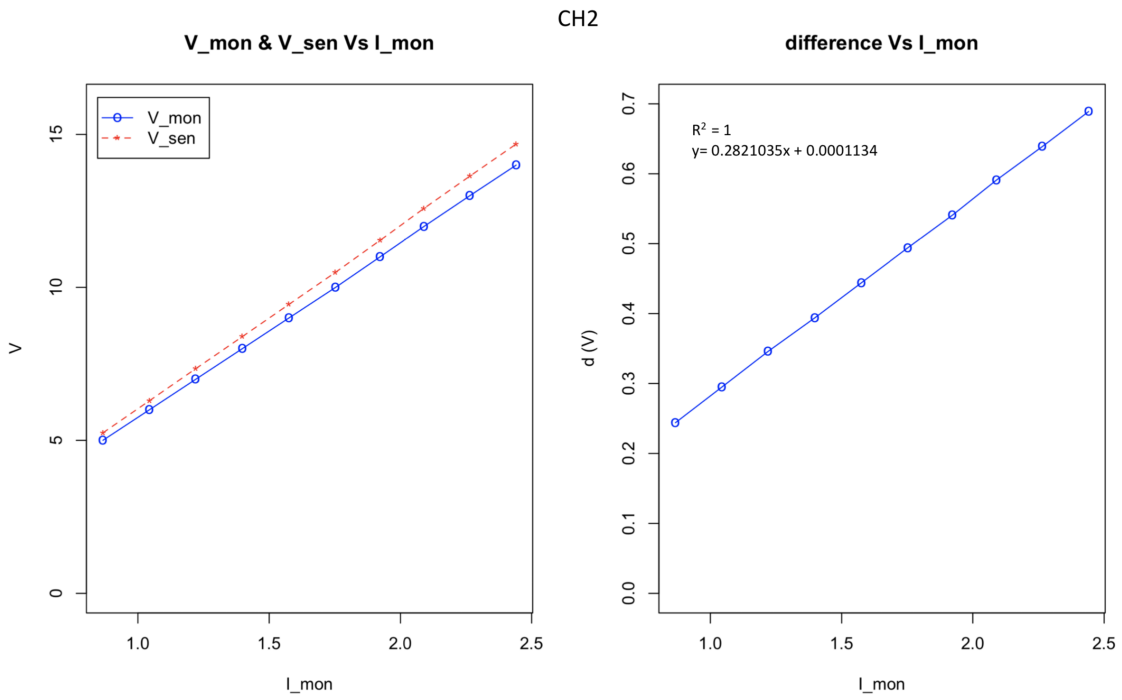

Figure 16: CH2

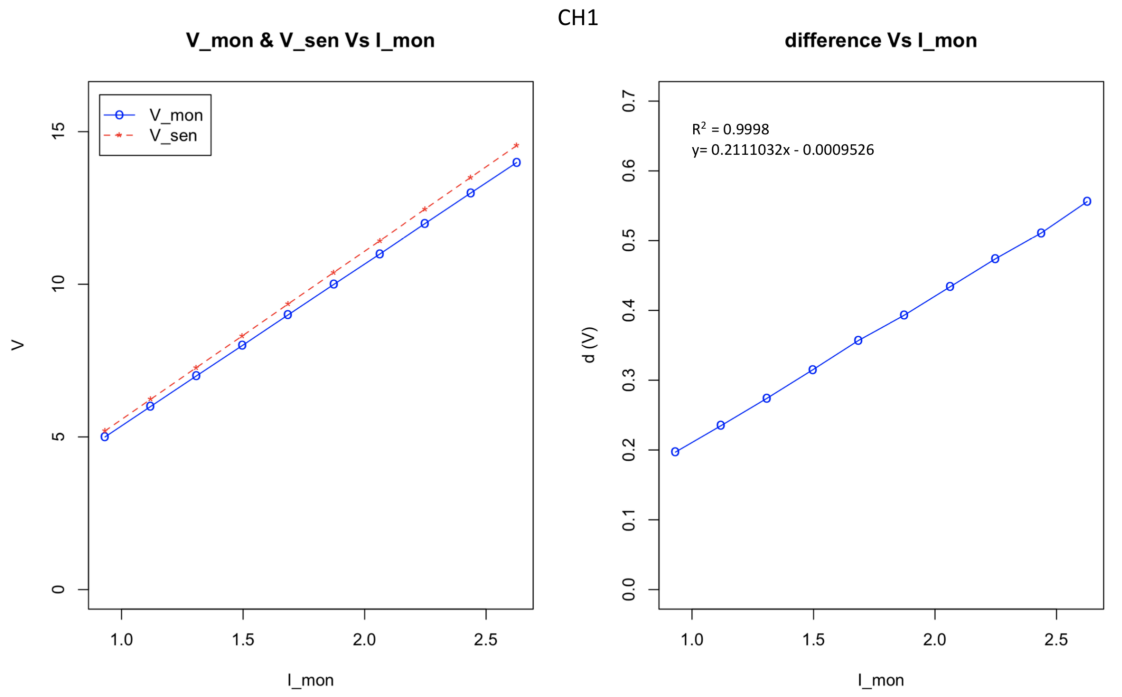

Figure 17: CH1

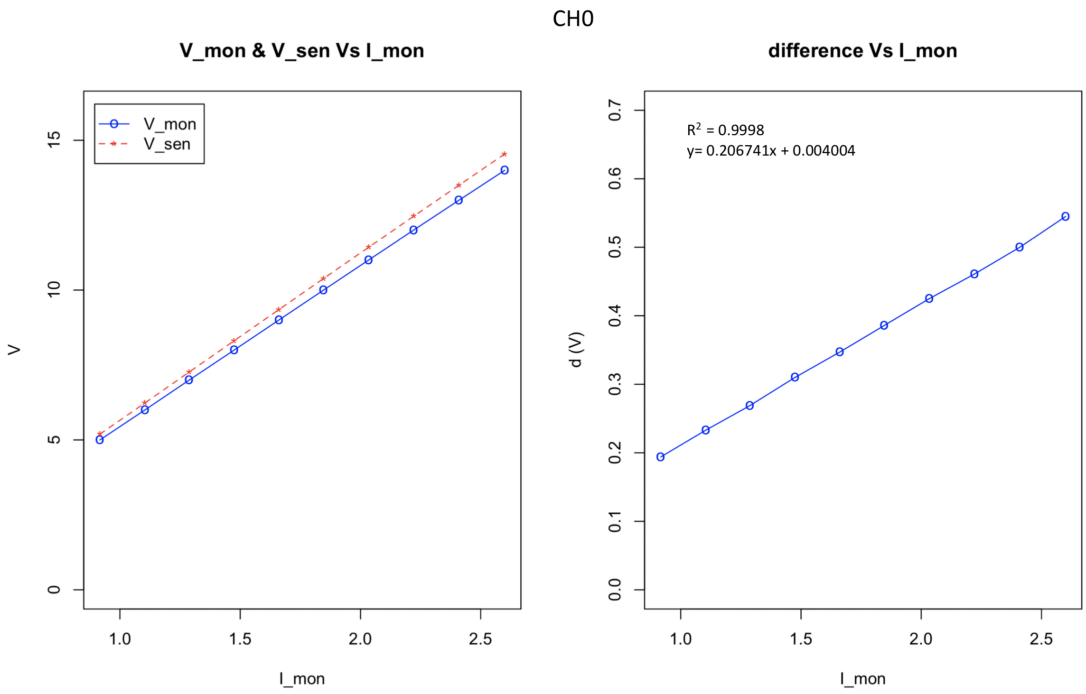

Figure 18: CH0

After the LV board was tested using a 6Ω resistance circuit, the resistance was lowered to 3.5Ω to test it for higher currents. This was done using only channels 0 and 3 due to time restriction and are shown below

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5.003	5.311	5.034	0.02717	1.445	0.92	0.994
6	6.001	6.375	6.041	0.032205	1.736	0.941	0.993
7	7.003	7.437	7.05	0.03725	2.029	0.942	0.993
8	8.001	8.585	8.12	0.0426	2.315	0.932	0.985
9	9.008	9.663	9.14	0.0477	2.606	0.932	0.986
10	10.001	10.73	10.16	0.0528	2.896	0.932	0.984
11	10.999	11.802	11.17	0.05785	3.186	0.932	0.985
12	12.005	12.888	12.19	0.06295	3.477	0.931	0.985

Table 10: CH3 higher current

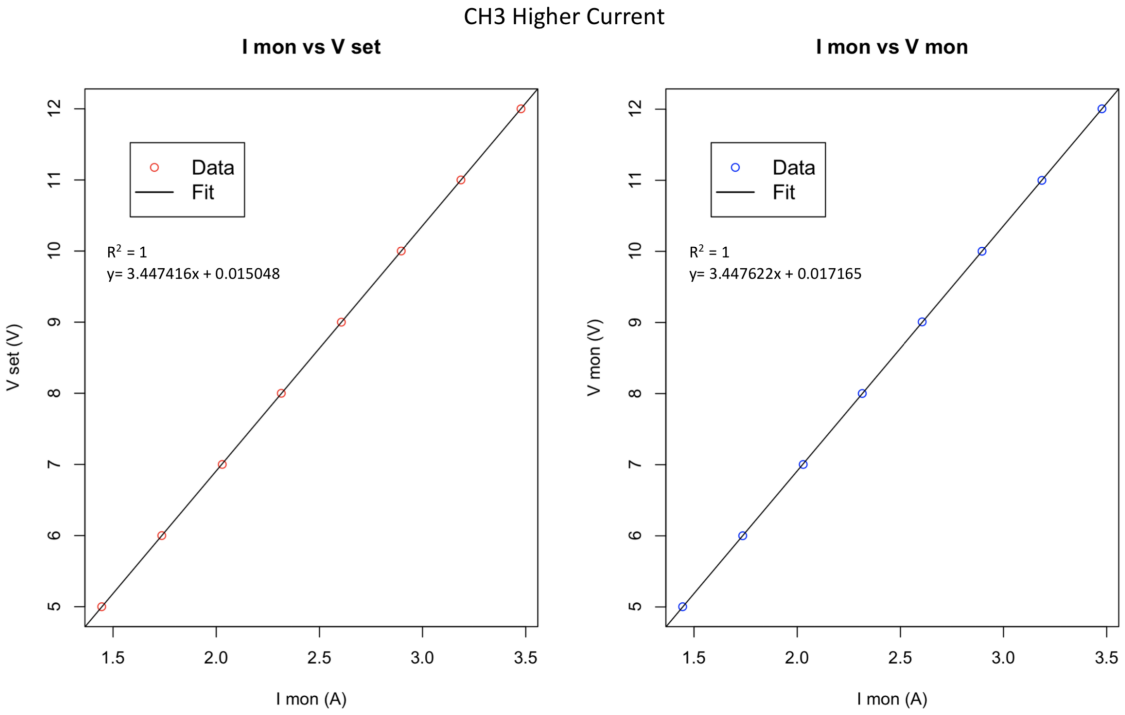

Figure 19: CH3 higher current

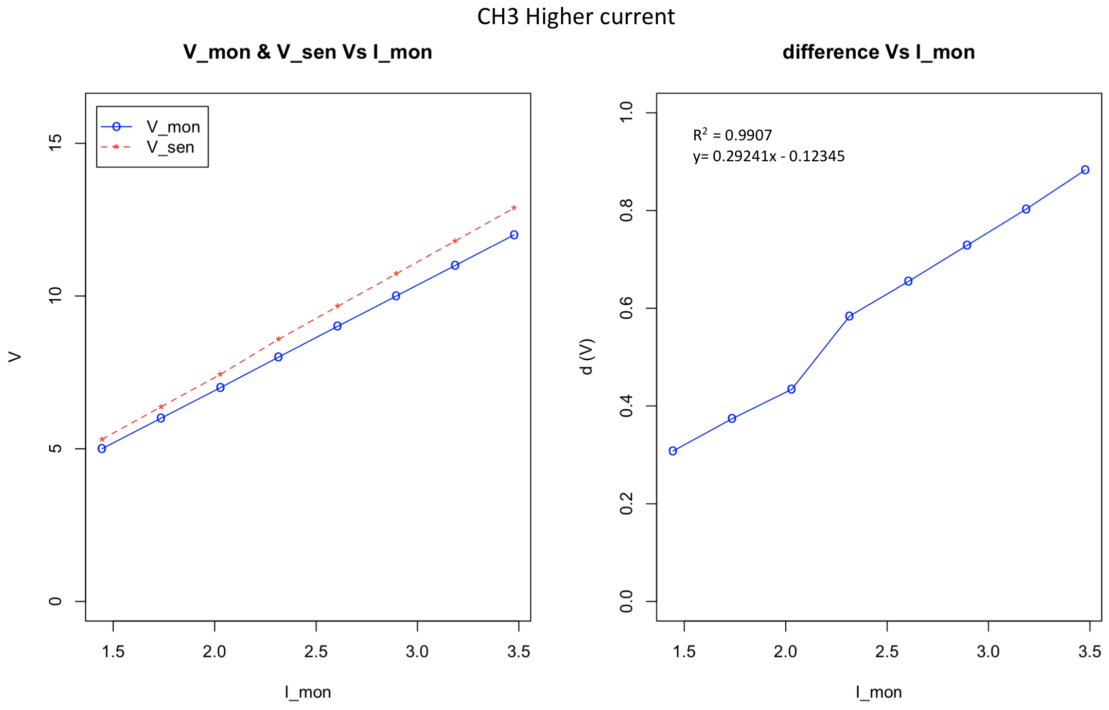

Figure 20: CH3 higher current

Vset (V)	Vmon (V)	Vsense (V)	Vmeter (V)	Vmeter Error (V)	Imon (A)	Vmon/Vsense	Vmon/Vmeter
5	5	5.313	5.046	0.02723	1.412	0.92	0.991
6	6.001	6.375	6.053	0.032265	1.693	0.941	0.991
7	6.999	7.436	7.06	0.0373	1.977	0.941	0.991
8	8.001	8.502	8.07	0.04235	2.265	0.941	0.991
9	9.002	9.566	9.08	0.0474	2.549	0.941	0.991
10	10.002	10.632	10.09	0.05245	2.844	0.941	0.991
11	11.002	11.694	11.1	0.0575	3.131	0.941	0.991
12	12.007	12.763	12.12	0.0626	3.418	0.941	0.991
13	13	13.821	13.12	0.0676	3.699	0.941	0.991

Table 11: CH0 higher current

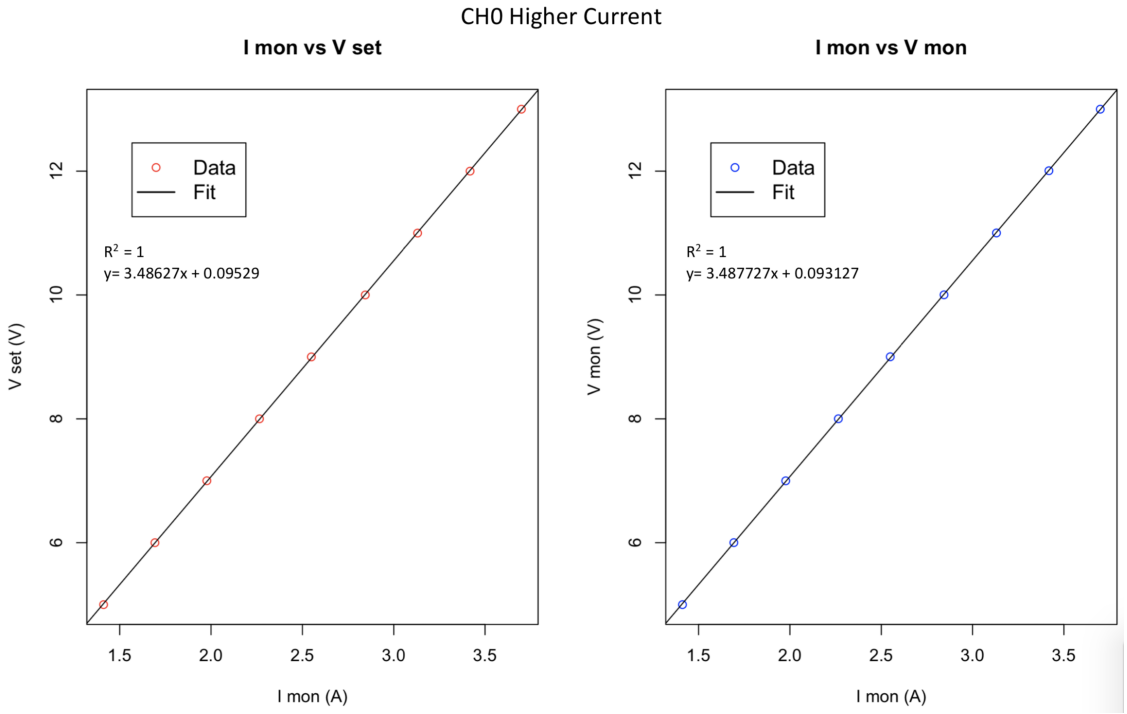

Figure 21: CH0 higher current

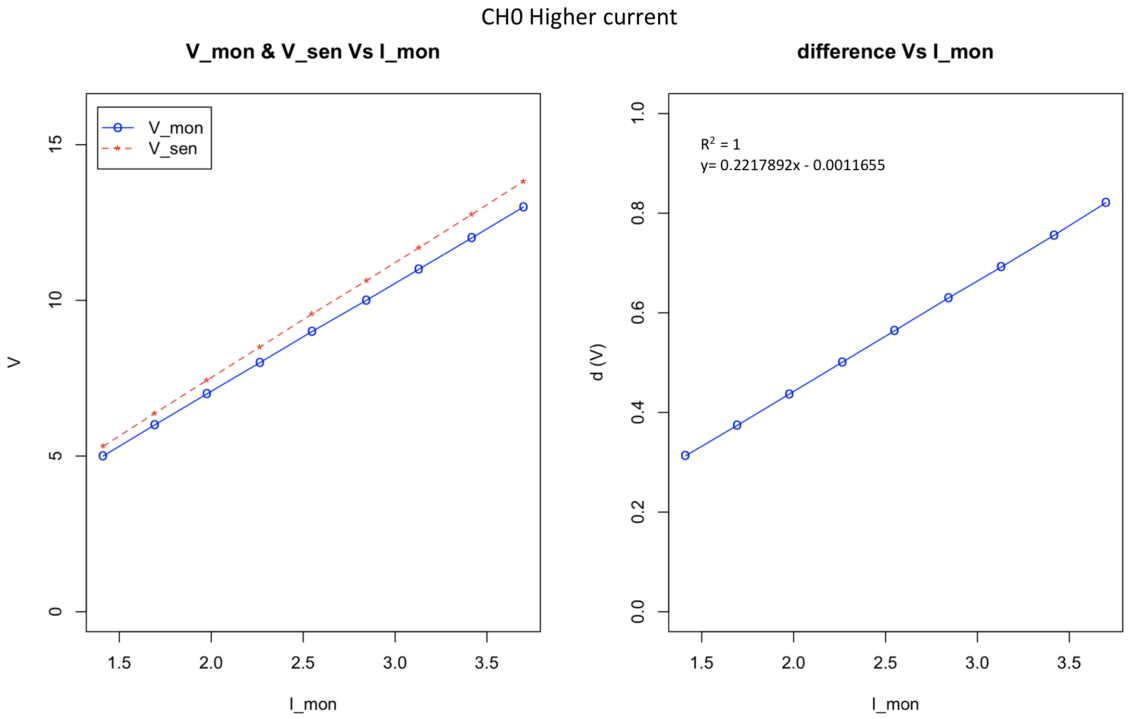

Figure 22: CH0 higher current

The resistance calculated from I-V curves for channels 0 and 3 with higher current is also shown below

CH	R (Vset)(Ohm)	R (Vmon) (Ohm
0	3.48627	3.487727
3	3.447416	3.447622

Table 12: Calculated resistance for channels 0 and 3 using the I-V curves

3 THGEM

Pictures of the new THGEM were taken and the hole sizes were measured under a microscope.

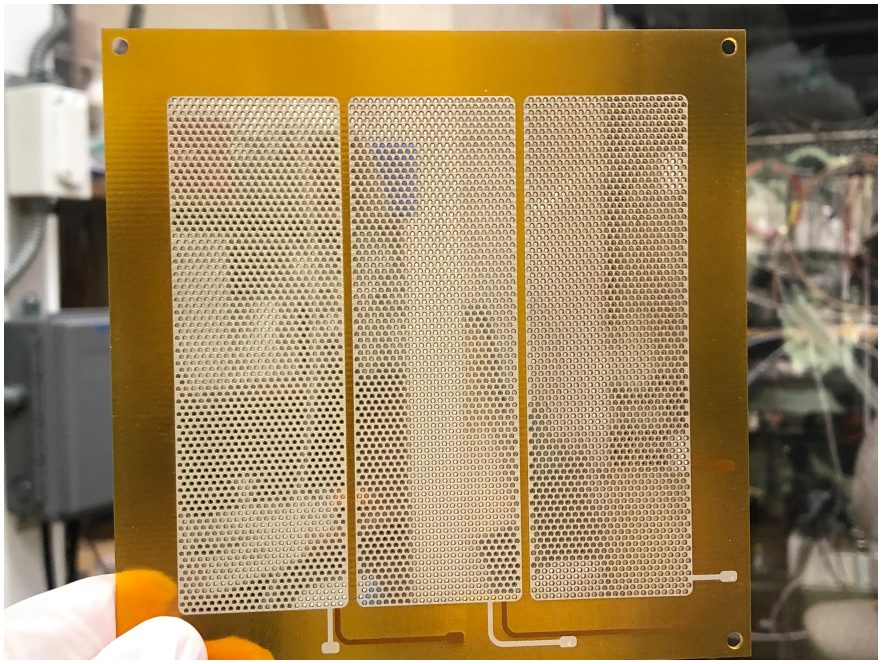

Figure 23: THGEM

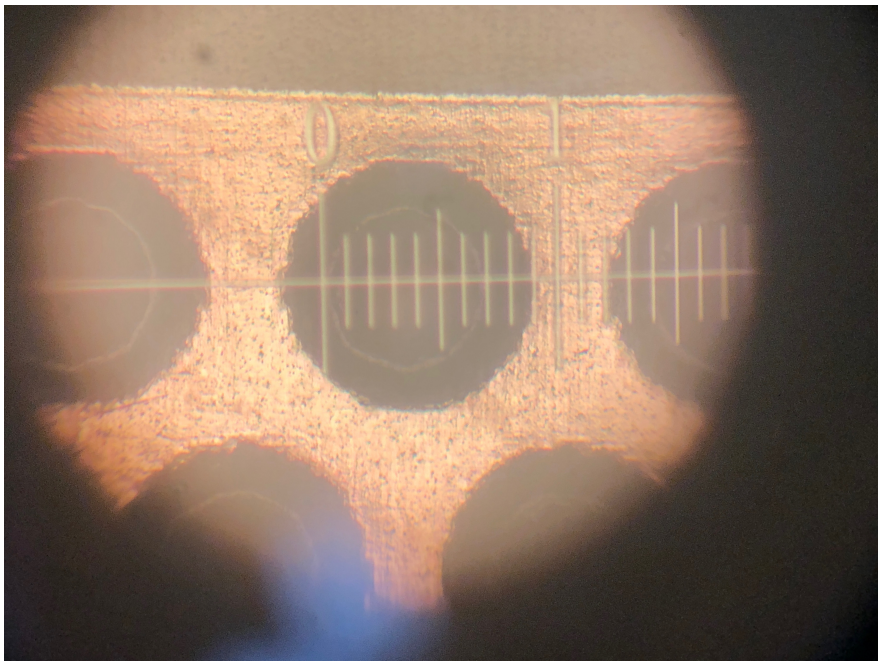

Figure 24: First sector: .7mm holes, .18mm rims

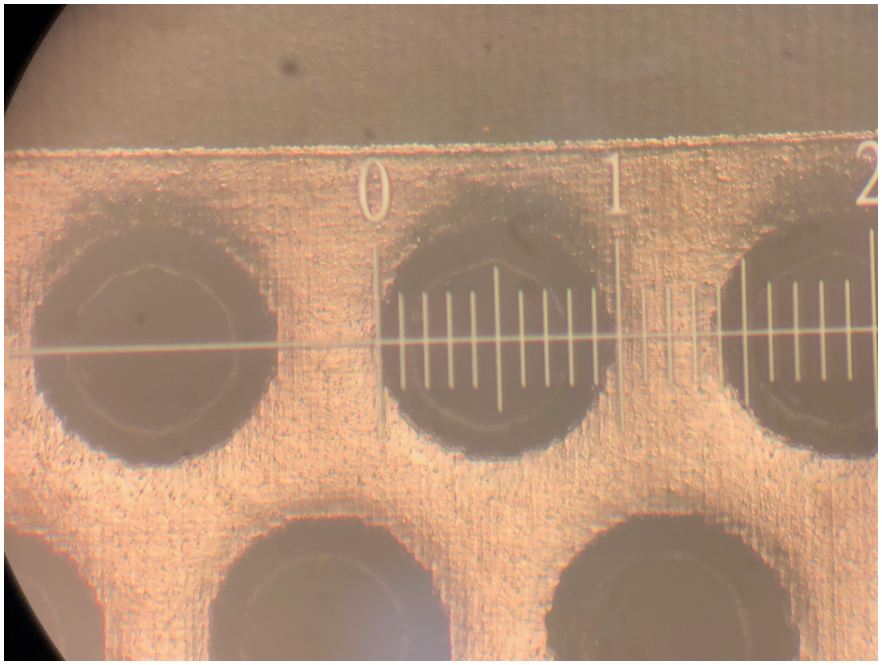

Figure 25: Middle sector: .7mm holes, .15mm rims

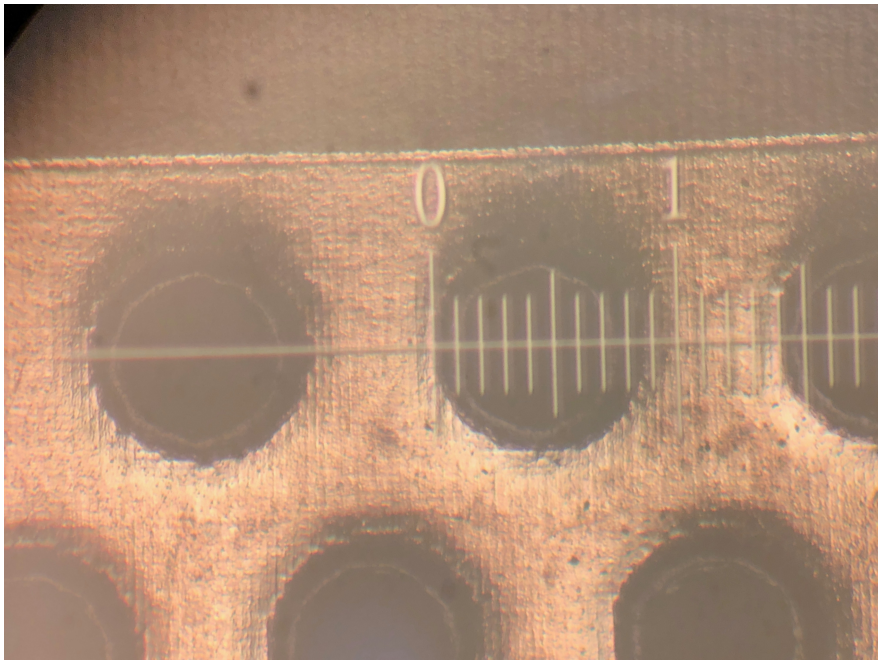

Figure 26: Last sector: .7mm holes, .1mm rims

4 PreAmp Test

A few preAmps were tested by observing their gain and duty cycles. The preAmps were connected to a signal generator and those signals were observed on an oscilloscope as shown below.

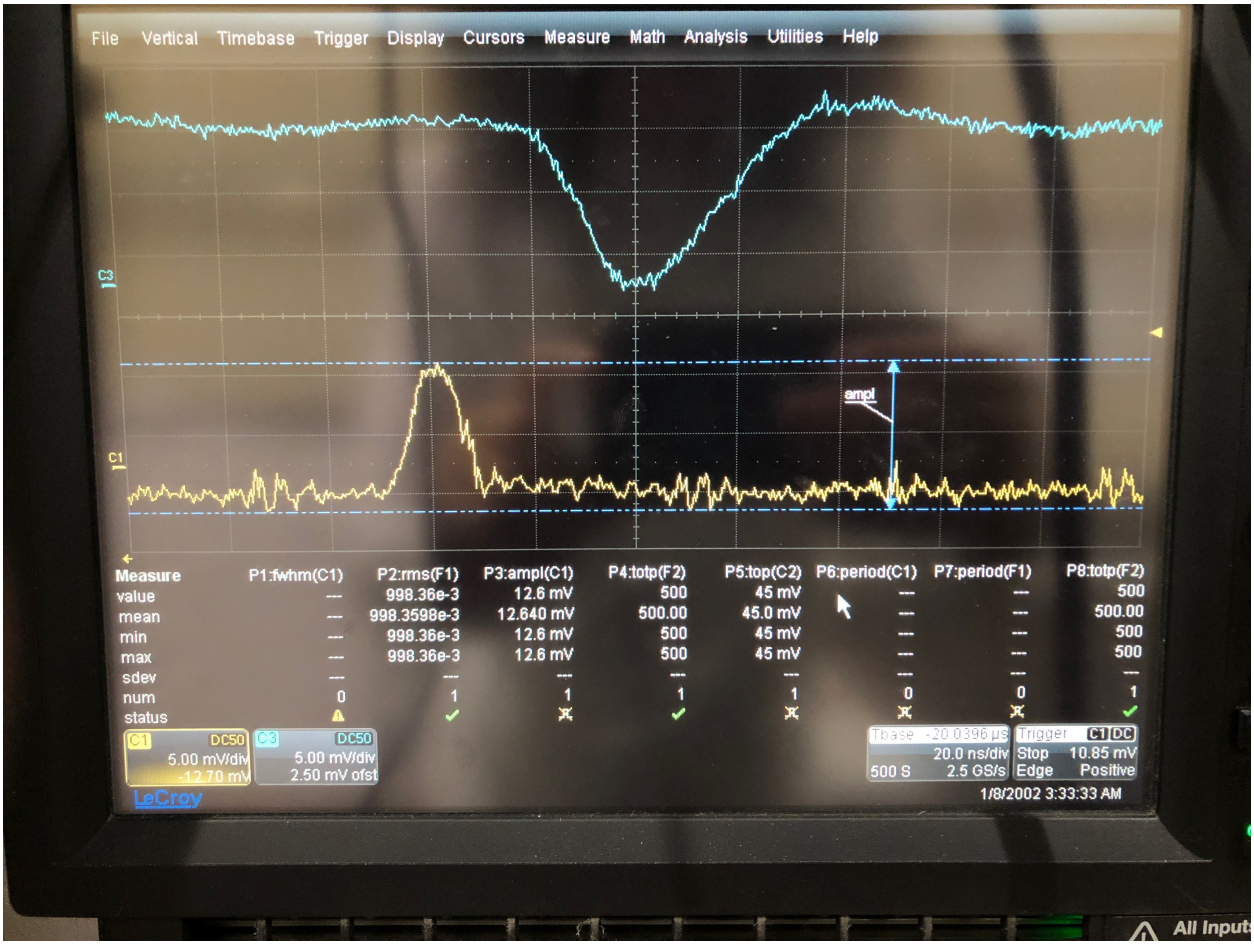

Figure 27: A working preAmp. The channel 1 signal (yellow) is the signal from the signal generator. The channel 3 signal (blue) is the signal after going through the preAmp.

After testing each preAmp it was discovered that some of them are in good condition while others don't work at all. The data for the preAmps were taken on Matt's flash drive since I was only helping him with the measurements and so I don't actually have them to present here.

5 Summary and Conclusions

The LV board was successfully tested using a simple 4 variable resistors circuit. The results of the test agree with expectations except for the large difference between the monitored voltage and the sense voltage which is due to some unknown reason. The THGEM measurements agree closely to the expected values from the original design. The PreAmps were tested and some were found to not work.