FEC Firmware Upgrade at Florida Tech

Adam Lastowka

April 20, 2023

1 Introduction

This document presents a technical guide to the firmware (FW) upgrade process for the Hohlmann Research Group's version 6 (v6) front-end converters (FECs). This upgrade was necessitated by the transition from our lab's data acquisition (DAQ) software to the MicroMegas DAQ (mmDAQ) software (SW) developed for ATLAS [3].

2 Hardware

Currently, Florida Tech has a total of 12 functional FECs. Three of these are v6 FECs[1], which can be upgraded for use with mmDAQ. FECs are a component of the scalable readout system (SRS), a readout system developed for laboratory use by CERN's RD51 collaboration [2].

FECs are typically situated in Eurocrates: powered crates that enable easy FEC transport and setup (shown in figure 1).

Version 6 and version 1.x FECs each have their own respective crates. However, the v1 crate's power cable can still fit snugly into v6 FECs. **Do not install a v6 FEC in the crate intended for v1 FECs.** Doing so will burn the v6 FEC's voltage regulator.

3 FW Installation

This section is largely based on the helpful guide written by Seulgi Kim [1].

3.1 Hardware Connections.

Installing FW (also referred to as "flashing") on a device requires writing to its programmable read-only memory (PROM). For FECs, this can be done with a Xilinx Platform Cable[2], and the associated Xilinx software, IMPACT[3]. Ensure that all peripherals (APVs and ADCs) are unplugged from the FEC. Then, Wwth the v6 FEC's eurocrate powered OFF, attach the Xilinx platform cable to the JTAG/J1 port on the FEC. Plug the other end into a PC with IMPACT installed.

With our lab's modified v6 Eurocrate, the FW installation may fail if more than one FEC is plugged into the crate's power supply. To avoid this, ensure that **only one FEC in the crate is powered** during the upgrade.

Next, power on the FEC. If everything is attached properly, the indicator LED on the Xilinx box should turn green.

[1] Of the remaining nine, eight are v1.1, and one is v1.0. Another v6 FEC is currently under repair.
[2] A small box with a USB input and set of wires leading to a 7x2 female pin header socket connector.
[3] FECs are built around a *field-programmable gate array* (FPGA), a configurable integrated circuit (IC) invented by Xilinx.

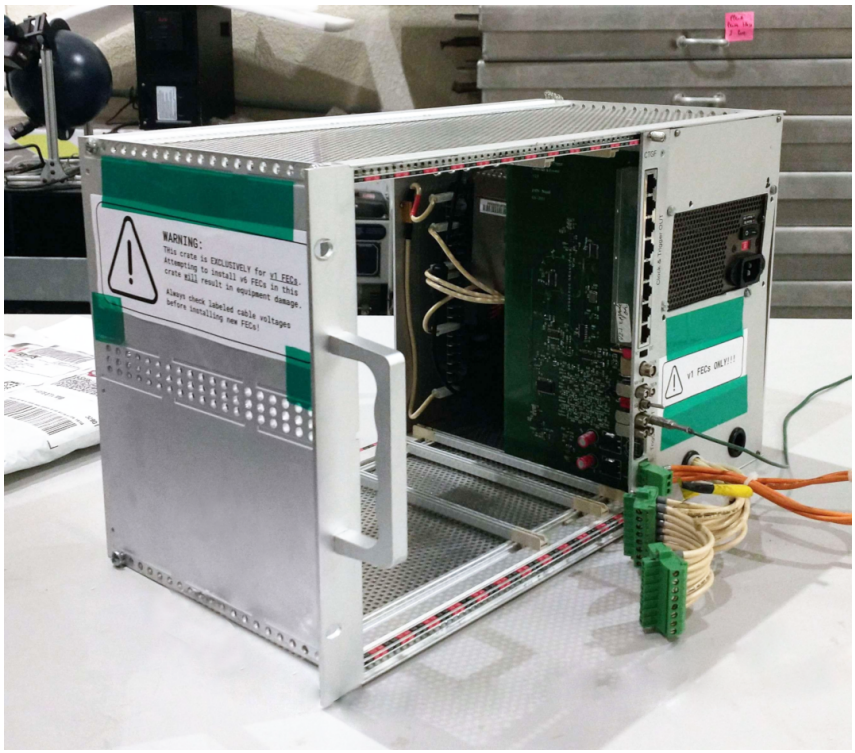

Figure 1: Our lab's v1 FEC Eurocrate

4 Using IMPACT

4.1 Environment Variable Modification

This step has already been performed on our lab's X-Ray PC.

In order to avoid an "ID check failed" error, IMPACT needs to know to skip ID checking. Unfortunately, this can only be done by setting (and creating, if necessary) the environment variable `XIL_IMPACT_SKIPIDCODECHECK` to 1. This process depends on the operating system of the PC. For OS-specific instructions, refer to the guide at [4].

4.2 Connecting to the FEC

Open IMPACT on the PC. Be sure to open the 64-bit version[4], or the installation may fail. When IMPACT opens, create a project by clicking "yes" on the dialog box. Next, accept the default setting (configure using JTAG boundary scan), and click "OK". The window should now show a device labeled "`xc6vlx130t bypass`" (shown in 2 with the message "Identify Succeeded" displayed in a blue box. Select "no" when asked to assign configuration files, then select "OK" to accept the default device programming properties[5].

4.3 Flashing the FEC

In IMPACT, right-click the blue dotted box labeled "`SPI/BPI?`" and select "Add SPI/BPI Flash". Select the `.mcs` file containing the new mmDAQ-compatible FW. [6]. In the new dialog box, select `SPI PROM` and `S25FL064P` as the PROM type[7]. Leave the data width parameter at its default.

[4]This procedure has not been tested on a 32-bit PC.
[5]Be sure that "verify" is checked to avoid false success messages.
[6]For this upgrade, the file name is `fecv6_adc_v1_0_33MH.mcs`
[7]For FECs manufactured after 2019, the proper PROM type is `MT25QL128ABA`

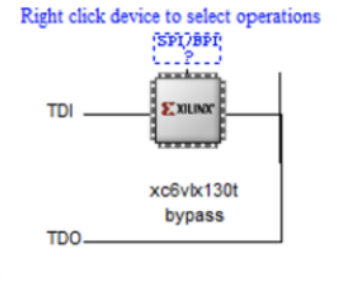

Figure 2: IMPACT should display this graphic upon successful identification of the FEC.

Finally, right-click the green box labeled "`FLASH`" and select "Program", then "OK". The process should take roughly ten minutes. If successful, the text "programmed successfully" should appear in the window.

5 Post-Upgrade Usage

Only one of the small form factor pluggable (SFP) ports on the FEC is usable. Post-upgrade, this port is the `J11` (bottom) port, as shown in figure 3.

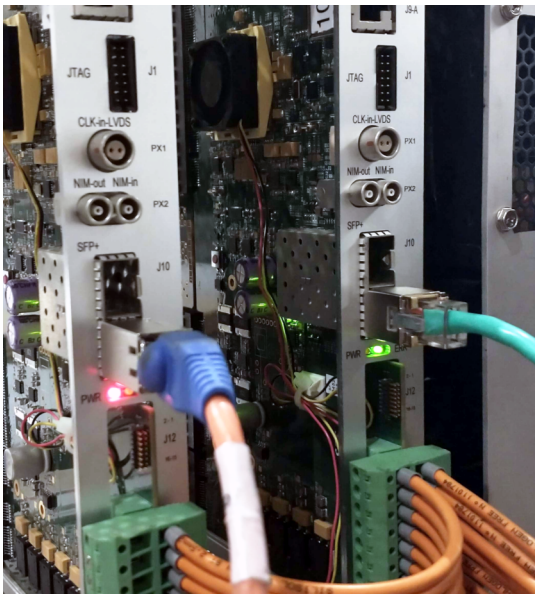

Figure 3: Two FW-upgraded FECs with plugs in their J11 SFP ports. The JTAG ports used for flashing are also visible.

Flashing the FEC should not change its IP address or basic functionality. Regardless, if the FEC IP is unknown, use the following command to send a broadcast ping:

```
ping -I [INTERFACE] -b 255.255.255.255
```

Where `[INTERFACE]` is the network interface card the FEC is attached to (`enp2s0` for our lab's DAQ PC). The FEC should respond with its IP displayed in the command output. Be sure that UDP jumbo frames are enabled on the interface; i.e. running `ifconfig [INTERFACE]` should show `mtu 9000`.

References

[1] Seulgi Kim, CERN, "FEC Firmware Upgrade for GE2/1 QC5," 2023.

[2] The RD51 Collaboration, "What is SRS: short introduction, status and outlook," 2010, https://indico.cern.ch/event/77597/contributions/2088463/attachments/1056845/1506857/RD51-SRS-Description.pdf.

[3] M. Byszewski, CERN, "MMDAQ Q&A," 2012, https://indico.cern.ch/event/218341/contributions/1519619/attachments/352429/491014/mmdaq_QA.pdf.

[4] AMD Xilinx, "11630 - Install - How do I check or manually set environment variables?", 2021, https://support.xilinx.com/s/article/11630?language=en_US.