Electronics Integration for the GE2/1 and ME0 GEM Detector Systems for the CMS Phase-2 Muon System Upgrade

Stephen D. Butalla & Marcus Hohlmann, On behalf of the CMS Muon Group
Florida Institute of Technology

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Introduction

With the projected five-fold increase in instantaneous luminosity resulting from the High Luminosity upgrade of the Large Hadron Collider, the CMS experiment is in the process of upgrading its muon spectrometer [1]. Two triple-Gas Electron Multiplier (GEM) detector systems—the GE2/1, currently in the early mass-production phase, and the ME0, currently in the prototyping phase—are undergoing frontend electronics integration. These detector systems follow the electronics path of the GE1/1, the first generation GEM detector system fully installed during the Phase-2 muon system upgrade of the CMS experiment. The GE2/1 detector system provides additional coverage between $1.62 < |\eta| < 2.43$, and the ME0 detector system increases coverage of the muon spectrometer between $2.0 < |\eta| < 2.8$ (see Fig. 1). Electronics integration efforts for the GE2/1 are carried out at: CERN, Rice University, Texas A&M, and Florida Tech; and for the ME0 at CERN, UCLA, and Florida Tech. This poster discusses the current status of the electronics integration effort on full-size chamber prototypes by the CMS GEM collaboration and the future prospects of the frontend electronics readout systems.

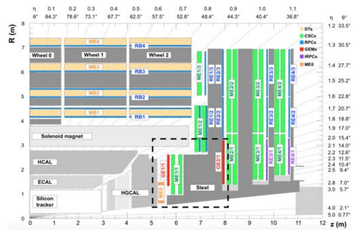

Figure 1: Quadrant of the CMS experiment with the GEM upgrade highlighted [1].

The GE2/1 and ME0 Detector Systems

The GE2/1 and ME0 are modular triple-GEM detector systems. Each GE2/1 chamber consists of four modules, namely the M5–M8 modules for the front GE2/1 chamber, and the M1–M4 modules for the back chamber [see Fig. 3 (left)]. When installed in the CMS experiment, a front chamber and back chamber will be mounted back-to-back, which will be installed in front of the ME2/1 cathode strip chamber in the second muon station (Fig. 1). The ME0 detector system consists of 6 individual modules stacked upon one another. These "stacks" will be inserted in the endcap nose.

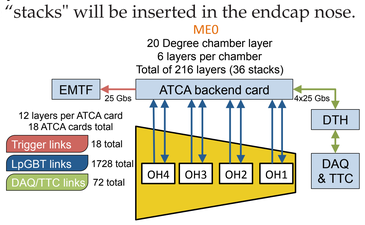

Figure 2: Block diagram of the frontend/backend electronics for the ME0.

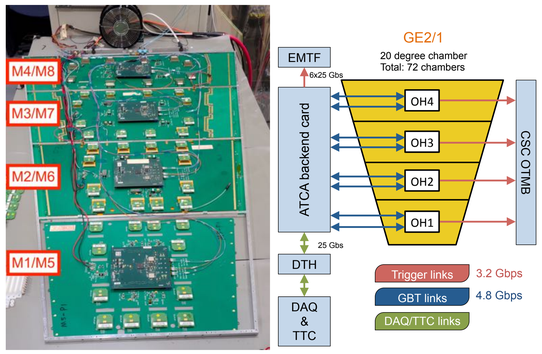

Figure 3: Full GE2/1 front chamber prototype with modules indicated (left) and block diagram of the frontend/backend GE2/1 electronics (right).

Frontend Electronics for the GE2/1 and ME0 Detector Systems

Figure 4: A GE2/1-M6 GEM electronics board with prototype frontend electronics.

Both the GE2/1 and ME0 detector systems share similar frontend electronics. For example, each GE2/1 module or ME0 layer will have a GEM electronics board (GEB), which is responsible for routing the signals from the readout (RO) application specific integrated circuits (ASICs) to the optohybrid (OH). The GEB is fixed to the detector readout board that the inputs of the frontend readout ASICs are plugged into. The OH is responsible for communication between the frontend and backend, transmitting both DAQ and trigger data via the versatile transreceiver (VTRx) and versatile twin transmitter (VTTx) on the GE2/1 OH, and the VTRx+ on the ME0 OH. The GE2/1 OH (Fig. 7) features a Xilinx Artix-7 FPGA, which interfaces with two gigabit transceiver ASICs (GBTs) and GBT-Slow Control Adapter (GBT-SCA) chipsets.

One notable difference is that the ME0 OH features 2 low-power GBT (LpGBT) chips in lieu of an FPGA due to the harsh radiation environment that the ME0 will operate in (Fig. 8). The frontend RO ASICs are the VFAT3b packaged in a plugin card (Fig. 6). Low voltage for the GE2/1 will be distributed by the FEASTMP_CLP DC-DC converter, while the ME0 will be powered by the bPOL12V DC-DC converters. One GE2/1 GEB is operated with one OH, which communicates with 12 VFATs, while one ME0 GEB (wide and narrow for the entire chamber) contains 2 OHs per GEB, each communicating with 6 VFATs a piece.

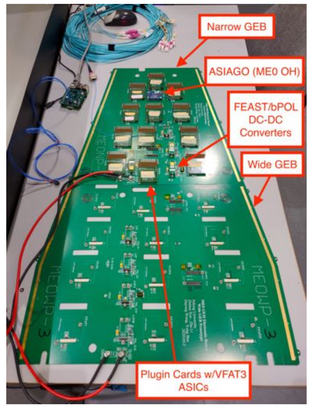

Figure 5: Wide and narrow ME0 GEBs.

Figure 6: The front (left) and back (right) of the plugin card with VFAT3b ASIC.

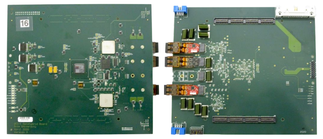

Figure 7: GE2/1 OH front (left) and back (right) [2].

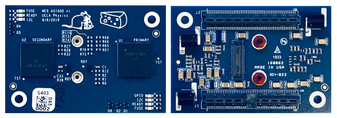

Figure 8: ME0 OH front (left) and back (right) [3].

Integration Testing

Frontend electronics integration for the GE2/1 and ME0 detector systems consists of several procedures and tests to establish communication, calibrate, and determine the noise in the system. For both detectors, the integration pipeline is identical, although there are some exceptions (e.g., since the ME0 OH doesn't have an FPGA, FPGA programming is skipped during the second step of the pipeline). See Tab. 1 for a list and explanation of the integration procedures.

Table 1: Frontend Electronics Procedure

Step	Procedure
0	Test the voltages produced by the DC-DC converters
1	Establish connectivity [check (Lp)GBT communication, check trigger links, program FPGA (GE2/1), GBT phase scans, check VFAT synchronization]
2	Retrieve VFAT calibration data from the database and program nominal register values
3	Calibrate the VFATs by performing digital-to-analog converter (DAC) scans to characterize and determine nominal values of programmable registers
4	Equivalent noise charge (ENC) measurement for DAQ eLink
5	S-bit noise measurement for trigger eLinks

Connectivity testing begins with first establishing communication with the OH, checking the trigger links, (programming the FPGA for GE2/1), and scanning the clock phases of the (Lp)GBTs to synchronize the VFATs to a common clock. Example output in Fig. 9 below shows successful results for ME0 phase scans.

```
phase : 0123456789ABCDEF
VFAT02: xx---x-xxxx+xxxx- (center=10, width=9) GOOD
VFAT03: x---xxxxx+xxxxx- (center=9, width=11) GOOD
VFAT10: xx---xxx+xx-xxxx- (center=7, width=6) GOOD
VFAT11: xx---xxxxx+xxxxx- (center=9, width=11) GOOD
VFAT18: xx---xxxxx+xxxxx- (center=9, width=11) GOOD
VFAT19: xx---xx-xxx+xxx-- (center=10, width=7) GOOD
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Figure 9: Phase scan results for the second OH on the wide ME0 GEB.

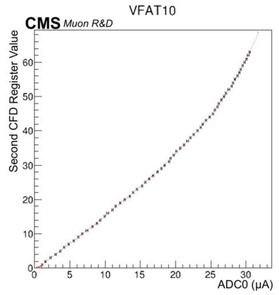

Figure 10: DAC characterization scan for the second constant fraction discriminator on a VFAT on a GE2/1-M7 module.

Next, the calibration data are retrieved from the CMS GEM database, which are subsequently programmed to the VFATs (e.g., the internal current and voltage biases). Characterization scans for each of the programmable DACs on each VFAT are performed by programming a register value and reading the output current or voltage by the analog-to-digital converter (ADC) to find the optimal value for each VFAT [see an example for the second constant fraction discriminator (CFD) below in Fig. 10 on a GE2/1 module]. This step ensures that each VFAT is properly calibrated, thus returning accurate data.

The noise present in the detector system must be understood (and minimized) to ensure uniform and reliable responses by each DAQ channel and trigger s-bit on each VFAT. Equivalent noise charge (ENC) measurements ("S-curves") are taken for the DAQ eLinks by injecting increasing amounts of charge into each channel and recording the comparator response, and then fitting a modified error function; see Eqn. 1 below:

$$f(q) = A \cdot \mathrm{erf}\left(\frac{\max(p,q) - \mu}{\sigma\sqrt{2}}\right) + A \tag{1}$$

where q is the magnitude of injected charge, $A = n/2$, where n is the number of injected charges, p is the pedestal (recorded comparator responses with no injected charge), μ is comparator threshold, and σ is the ENC derived from the function fit. S-curve results for a few channels are shown in Fig. 8 (left), the ENC distribution for 6 VFATs is shown in Fig. 11 (right), and S-curves for all 128 channels on one VFAT are shown in Fig. 12 (left).

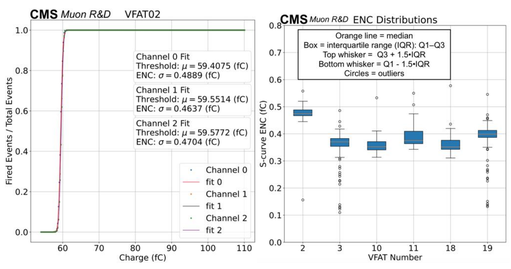

Figure 11: S-curves for a few channels with fit data (left). S-curve sigma (ENC) distributions for all 128 channels for 6 VFATs on an ME0 GEB (right).

The last step is the noise measurement for the trigger eLinks. For triggering purposes, the RO strips (connected to a VFAT) are paired, resulting in 64 strip groups, or "S-bits." When one (or both) of the two strips is (are) triggered, an S-bit is recorded. To determine the noise, first the threshold is fixed, and one by one each S-bit is unmasked and counts are recorded. This is repeated for the entire DAC range of $[0, 255]$.

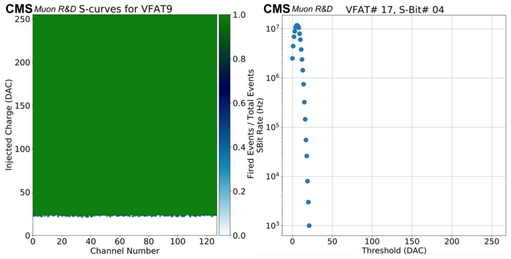

Figure 12: S-curves for all channels (left) and trigger S-bit noise rate measurement (right) for a single S-bit on one VFAT on an ME0 detector.

GE2/1 and ME0 Electronics Integration Status and Plans

With the GE2/1 prototype electronics integration efforts by the GEM collaboration coming to a close, mass production of the GE2/1 GEM detectors has been initiated. All electronic components for GE2/1 will be manufactured and tested by February of 2022, and full electronics integration with manufactured chambers completed by February of 2023 for both endcaps. The ME0 electronics integration effort is currently underway, with test stands testing components and integrating electronics on chambers at CERN, UCLA, and FIT. Recently, the second version preproduction OH was approved for manufacturing, and will begin production once the version 1 LpGBTs arrive. The ME0 GEB is also in its final prototyping stages, which will soon be reviewed and approved for production. The collaboration is currently testing the X2O ATCA backend card with various FPGAs and optics, with a final design ready by early 2022. Manufacturing and testing of the ME0 on-chamber electronics is projected to be completed by November 2022, with all detector stacks installed in the new nose by February 2026.

Acknowledgements

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References

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[2] CMS GEM Collaboration, "The CMS GEM Endcap Station 2 Ring 1 (GE2/1) OptoHybrid Board," https://twiki.cern.ch/twiki/bin/viewauth/CMS/GE21OHBoardTwiki.

[3] CMS GEM Collaboration, "The ME0 Optohybrid Board (ASIAGO)," https://twiki.cern.ch/twiki/bin/view/CMS/ME0ASIAGO.