**Introduction**

With the projected five-fold increase in instantaneous luminosity resulting from the High Luminosity upgrade of the Large Hadron Collider, the CMS experiment is in the process of upgrading its muon spectrometer [1]. The triple-Gas Electron Multiplier (GEM) detector systems—the GE2/1, currently in the early mass-production phase, and the ME0, currently in the prototyping phase—are undergoing front-end electronics integration. These detector systems follow the electronics path of the GE1/1, the first generation GEM detector system installed during the Phase-2 muon system upgrade of the CMS experiment. The GE2/1 detector system provides additional coverage of the muon spectrometer between 2.8 < |η| < 2.8 (see Fig. 1). Electronics integration efforts for the GE2/1 are carried out at CERN, Rice University, Texas A&M, and Florida Tech, and for the ME0 at CERN, UCLa, and Florida Tech. This poster discusses the current status of the electronics integration effort on full-size chamber prototypes by the CMS GEM collaboration and the future prospects of the front-end electronics readout systems.

**The GE2/1 and ME0 Detector Systems**

The GE2/1 and ME0 are modular triple-GEM detector systems. Each GE2/1 chamber consists of four modules, namely the M5–M8 modules for the front GE2/1 chamber, and the M1–M4 modules for the back chamber (see Fig. 3 [left]). When installed in the CMS experiment, a front chamber and back chamber will be mounted back-to-back, which will be installed in front of the ME2/1 cathode strip chamber in the second muon station (Fig. 1). The ME0 detector system consists of 6 individual modules stacked upon one another. These "stacks" will be inserted in the endcap.

**Frontend Electronics for the GE2/1 and ME0 Detector Systems**

Both the GE2/1 and ME0 detector systems share similar front-end electronics. For example, each GE2/1 module or ME0 layer will have a GEM electronics board (GEB), which is responsible for routing the signals from the electronics. For example, each GE2/1 module or ME0 layer will have a GEM electron multipliers—typically eight GEM modules—on one side of the module and a GEM compatible interface card (GCI) on the other side. The GEB communicates with 12 VFATs, while the VFAT communicates to the LpGBT for the entire chamber) contains 2 OH1 and 2 OH2 for a single S-bit on one VFAT on an ME0 detector.

**Frontend electronics integration for the GE2/1 and ME0 detector systems consists of several procedures and tests to establish communication, calibrate, and determine the noise in the system. For both detectors, the integration pipeline is identical, although there are some exceptions (e.g., since the ME0 OH doesn’t have an FPGA, FPGA programming is skipped during the second step of the pipeline). See Tab. 1 for a list and explanation of the integration procedures.**

**Integration Testing**

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**Figure 1:** Quadrant of the CMS experiment with the GEM upgrade highlighted [1].

**Figure 2:** Block diagram of the frontend/backend electronics for the GE2/1.

**Figure 3:** Full GE2/1 front chamber prototype with modules indicated (left) and block diagram of the frontend/backend GE2/1 electronics (right).

**Figure 4:** A GE2/1-M6 GEM electronics board with prototype front-end electronics.

**Figure 5:** Wide and narrow ME0 GEBs (GBT-SCA) chips.

One notable difference is that the ME0 OH features 2 low-power GBT (LGBT) chips in lieu of an FPGA due to the harsh radiation environment that the ME0 will operate in (Fig. 8). The front-end RO ASICs are the VFATs, packaged in a plug-in card (Fig. 6). Loss voltage for the VFAT is distributed by the FEAST-CLP DC-DC converter, while the ME0 will be powered by the LPVC 12V DC-DC converters. One GE2/1 GEB is operated with one OH, which communicates with 12 VFATs, while one ME0 GEB (wide and narrow for the entire chamber) communicates with 6 VFATs per GEB, each communicating with 6 VFATs per card.

**Figure 6:** The left (front) and back (right) of the plug-in card with VFATs-ASIC.

**Figure 7:** GE2/1 OH front (left) and back (right) [2].

**Figure 8:** ME0 OH front (left) and back (right) [3].

**Figure 9:** Phase scan results for the second OH on the wide ME0 GEB.

**Figure 10:** DAC characterization scan for the second construction fraction discriminator on a VFAT on a GE2/1-L7 module.

**Figure 11:** 5-curves for a few channels with fit data (left). 1-curve sigmas (ENC) distributions for all 128 channels on 6 VFATs on an ME0 GEB (right). The last step is the noise measurement for the trigger eLinks. For triggering purposes, the two strip groups, or "S-bits," are recorded. To determine the noise, the first threshold is fixed, and the second threshold is stepped in 0.1 eV steps, recording one count for each step. This step ensures that each VFAT is properly calibrated, thus returning accurate data.

**GE2/1 and ME0 GEM Electronics Integration Status and Plans**

With the GE2/1 prototype electronics integration efforts by the GEM collaboration coming to a close, mass production of the GE2/1 detector systems is in progress with the ME0 detector systems following. Both detector systems are undergoing front-end electronics integration. These detector systems follow the electronics path of the GE1/1, the first generation GEM detector system installed during the Phase-2 muon system upgrade of the CMS experiment. The GE2/1 detector system provides additional coverage of the muon spectrometer between 2.8 < |η| < 2.8 (see Fig. 1). Electronics integration efforts for the GE2/1 are carried out at CERN, Rice University, Texas A&M, and Florida Tech, and for the ME0 at CERN, UCLa, and Florida Tech. This poster discusses the current status of the electronics integration effort on full-size chamber prototypes by the CMS GEM collaboration and the future prospects of the front-end electronics readout systems.

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**References**