**Electronics Integration for the GE2/1 and ME0 GEM Detector Systems for the CMS Phase-2 Muon System Upgrade**

**Stephen D. Butalla & Marcus Hohlmann, On behalf of the CMS Muon Group**

**Florida Institute of Technology**

**POSTERS@LHC**

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**INTRODUCTION**

With the projected five-fold increase in instantaneous luminosity resulting from the High Luminosity upgrade of the Large Hadron Collider, the CMS experiment is in the process of upgrading its muon spectrometer [1]. Two triplet-Gas Electron Multiplier (GEM) detector systems—the GE2/1, currently in the early mass production phase; and the ME0, currently in the prototyping phase—are undergoing electronics integration. These detector systems follow the electronics path of the GE1/1, the first generation GEM detector system fully installed during the Phase-2 muon system upgrade of the CMS experiment. The GE2/1 detector system provides additional coverage between 1.62 < |η| < 2.4, and the ME0 detector system increases coverage of the muon spectrometer between 2.4 < |η| < 2.8 (see Fig. 1). Electronics integration efforts for the GE2/1 are carried out at CERN, Rice University, Texas A&M, and Florida Tech, and for the ME0 at CERN, UCLA, and Florida Tech. This poster discusses the current status of the electronics integration effort on full-size chamber prototypes by the CMS GEM collaboration and the future prospects of the front-end electronics readout systems.

**THE GE2/1 AND ME0 DETECTOR SYSTEMS**

The GE2/1 and ME0 are modular triplet-GEM detector systems. Each GE2/1 chamber consists of four modules, namely the M5–M8 modules for the front GE2/1 chamber, and the M1–M4 modules for the back chamber (see Fig. 3, left). When installed in the CMS experiment, a front chamber and back chamber will be mounted back-to-back, which will be installed in front of the ME2/1 cathode strip chamber in the second muon station (Fig. 1). The ME0 detector system consists of 16 individual modules stacked upon one another. These “stacks” will be inserted in the endcap nose.

**FRONTEND ELECTRONICS FOR THE GE2/1 AND ME0 Detector Systems**

Both the GE2/1 and ME0 detector systems share similar frontend electronics. For example, each GE2/1 module or ME0 layer will have a GEM electronics board (GEB), which is responsible for routing the signals from the readout (ROC) application specific integrated circuits (ASICs) to the opto-hybrid (OH). The GEB is fixed to the detector readout board that the inputs of the front-end ROC ASICs are plugged into. The OH is responsible for communication between the front-end and back-end, transmitting both DAQ and trigger data via the versatile transceiver (VTXs) and versatile twin transmitter (VTTs) to the GE2/1 OH and the VTTs on the ME0 OH. The GE2/1 OH (Fig. 7) features a Xinlin Artix-7 FPGA, which interfaces with two gigabit transceiver ASICs (GTBs) and GBT-S Low Power Control Adapter (GRT-S-CA) chips. One notable difference is that the ME0 OH features 2 low-power GBT (LGBT) chips in lieu of an FPGA due to the harsh radiation environment that the ME0 will operate in (Fig. 8). The front-end ROC ASICs are VFA1, packaged in a plug-in card (Fig. 6). Low voltage for the GE2/1 will be distributed by the FEAST_CPL DC-DC conver- vter, while the ME0 will be powered by the IXPEL2 DC-DC con- ververs. One GE2/1 GEB is op- erated with one OH, which com- municates with 12 VFA1s, while one ME0 GEB (wide and narrow for the entire chamber) contains 2 OHs per GEB, each communicat- ing with 6 VFA1s apiece.

**GE2/1 and ME0 Electronics Integration Status and Plans**

With the GE2/1 prototype electronics integration efforts by the GEM collaboration coming to a close, mass production of the GE2/1 GEM detectors is underway. All electronic components for GE2/1 will be manufactured and tested by late 2022, and full electronics integration with manufactured chambers completed by February of 2023 for both endcaps. The ME0 GEB is also in its final prototyping stages, which will soon be reviewed for mass production. The collaboration is currently testing the X0A ATCA backcard with various FC-PGA and optics, with a final design ready by early 2023. Manufacturing and testing of the ME0 on-chamber electronics is projected to be completed by November 2022, with all detector stacks installed in the new detector in February 2023.

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**REFERENCES**


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**INTEGRATION TESTING**

Frontend electronics integration for the GE2/1 and ME0 detector systems consists of several procedures and tests to establish communication, calibrate, and determine the noise in the system. For both detectors, the integration pipeline is identical, although there are some exceptions (e.g., since the ME0 OH doesn’t have an FPGA, FPGA programming is skipped during the second step of the pipeline). See Tab. 1 for a list and explanation of the integration procedures.

**Table 1: Frontend Electronics Procedure**

<table>
<thead>
<tr>
<th>Step</th>
<th>Procedure</th>
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<tbody>
<tr>
<td>1</td>
<td>Establish connectivity (check if LGBT communication, check trigger links, program FPGA (GE2/1), GBT phase scan, check VFA1 synchronization)</td>
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<tr>
<td>2</td>
<td>Connect the VFA1s by performing digital-to-analog converter (DAC) scans to characterize and determine nominal values of programmable registers</td>
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<tr>
<td>3</td>
<td>Noisy DAC characterization: check ENC measurement for DAC links</td>
</tr>
<tr>
<td>4</td>
<td>S-bit measurement for trigger eLinks</td>
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</tbody>
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**Figure 1: Quadrant of the CMS experiment with the GEM upgrade highlighted [1]**

**Figure 2: Block diagram of the front-end/back-end electronics for the ME0.**

**Figure 3: Full GE2/1 front chamber prototype with modules indicated (left) and block diagram of the front-end/back-end GE2/1 electronics (right).**

**Figure 4: A GE2/1-M6 GEM electronics board with prototype frontend electronics.**

**Figure 5: DAC characterization scan for the second constant fraction discriminator on a VFA1 on a GE2/1-I7 module.**

**Figure 6: The front (left) and back (right) of the plug-in card with VFA1-ASG.**

**Figure 7: GE2/1 OH front (left) and back (right) [2].**

**Figure 8: ME0 OH front (left) and back (right) [3].**

**Figure 9: Phase scan results for the second OH on the wide ME0 GEB.**

**Figure 10: DAC characterization scan for the second constant fraction discriminator on a VFA1 on a GE2/1-I7 module.**

**Figure 11: S-curves for a few channels with fit data (left) S-curve sigma (ENC) distributions for all 128 channels for 6 VFA1s on an ME0 GEB (right).**

**Figure 12: S-curves for a few channels (left) and trigger S-bit noise rate measurement (right) for a single S-bit on one VFA1 on an ME0 detector.**

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**Glossary**

- **DAC** (Digital to Analog Converter): An electronic device that converts digital signals into analog signals.
- **FPGA** (Field-Programmable Gate Array): An integrated circuit designed to be configured by a developer after manufacturing, rather than being programmed by the manufacturer.
- **GVTs** (Versatile Transceivers): ICs that provide interface for backend electronics.
- **VTNCs** (Versatile Transceiver Nuclei): Core of GVTs that provides interface for backend electronics.
- **OHs** (Optohybrids): Board that supplies power and communicates with front-end electronics.