FLORIDA TECH
MH

Highlights from GEM Phase 2 Upgrade Workshop

M. Hohlmann

FIT

5/25/2020

General Muon Meeting

GEM Workshops – Spring 2020

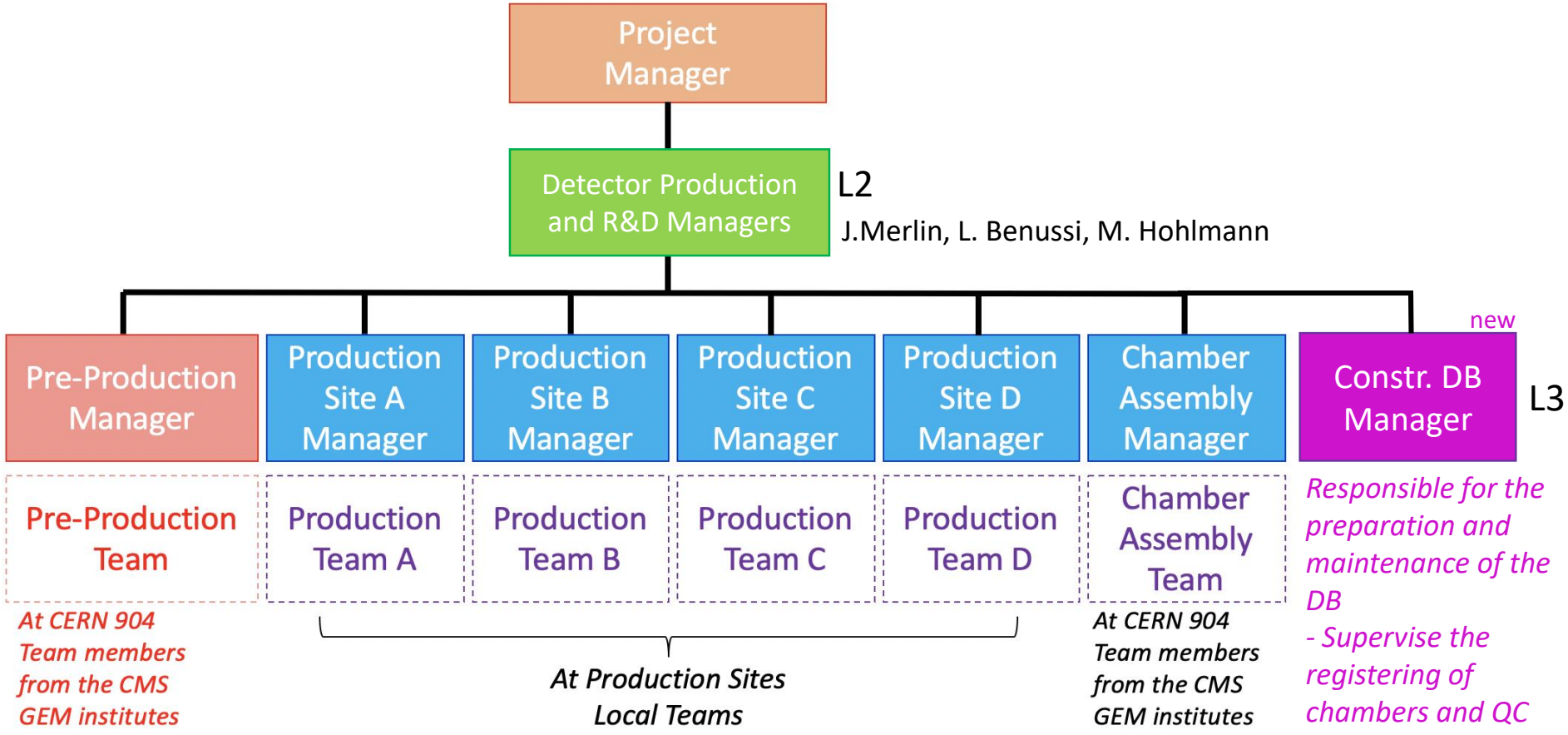
GEM Community is organizing a series of workshops:

- Phase 2 Upgrade May 18-20 (this summary)
  https://indico.cern.ch/event/918611/overview
  - Production and R&D
  - Electronics & DAQ
  - Technical Coordination
  - Mangement & Project planning
- Run Coordination June 3-4
- GE1/1 June 8-12

Detector Production and R&D

ME0 prototyping status, plans and related R&D	*Michele Bianco*	
CERN	06:30 - 06:50	
Rate capability measurements	*Francesco Fallavollita*	
CERN	06:50 - 07:10	
Plans for aging tests	*Dr Inseok Yoon*	
CERN	07:10 - 07:25	
Plans for discharge studies and neutron tests	*Davide Fiorina*	
CERN	07:25 - 07:45	
R&D Session: Coffee Break		
CERN	08:45 - 09:00	
X-talk studies with VFAT3	*Jeremie Alexandre Merlin*	
CERN	09:00 - 09:25	
X-talk studies with pulser & remaining R&D	*Stephen Butalla*	
CERN	09:25 - 09:55	
X-talk model	*Marcus Hohlmann*	
CERN	09:55 - 10:25	
Background simulation results	*Piet Verwilligen*	
CERN	10:25 - 10:50	
Test beam proposal for 2021	*Piet Verwilligen*	
CERN	10:50 - 11:10	

Organigram



Manager names and contact info available on the GE21 twiki page:
https://twiki.cern.ch/twiki/bin/viewauth/CMS/GE21DetectorProduction

GE2/1 Production in Peking Univ. (PKU) – new site

Site Manager: *Yong BAN, Dayong Wang(deputy)*

Status of the test setups	N_2 box for QC2	QC3	QC4	QC5 effective gain	QC5 uniformity	Comments
	Available and operational	Available and operational	Available and operational	Available and operational	Available at CERN	

Manpower status	Physicists	Technicians	Students
	4	1	5

Expected manpower situation in 2021:

Yong BAN (Professor)
Dayong WANG (Associate Professor)
Hongji MA: Senior Engineer
Aera JUNG: Postdoc
Meng LU: Postdoc
Chuqiao JIANG (PhD student)
Licheng Zhang (PhD student)
Xuelong QIN (PhD student, CERN-based for QC5-2)
+ another 2-3 master/PhD students

Expected max. rate of production*: 8 module/month*

PCB Production at Micropack

Producer: Micropack, based in India

Item	Quantity needed	Quantity ordered	Quantity received	Quantity tested
DRIFT M1 to M8	36	40	0	0
RO M1 to M8	36	40	0	0

Current Status: funding secured for pre-production: 4 sets (DRIFT+RO) for M1 to M6
Total : 24 DRIFT + 24 RO (7.5 % of the total production), expected to be available in Aug 2020

Internal review: to be organized after the reception of the first prototypes
https://twiki.cern.ch/twiki/bin/view/CMS/ReviewIndia (draft agenda)

Pending issues: Availability of funding for the remaining quantities. Investigations are on-going with Indian representatives

GE2/1 Production Preparation - Summary

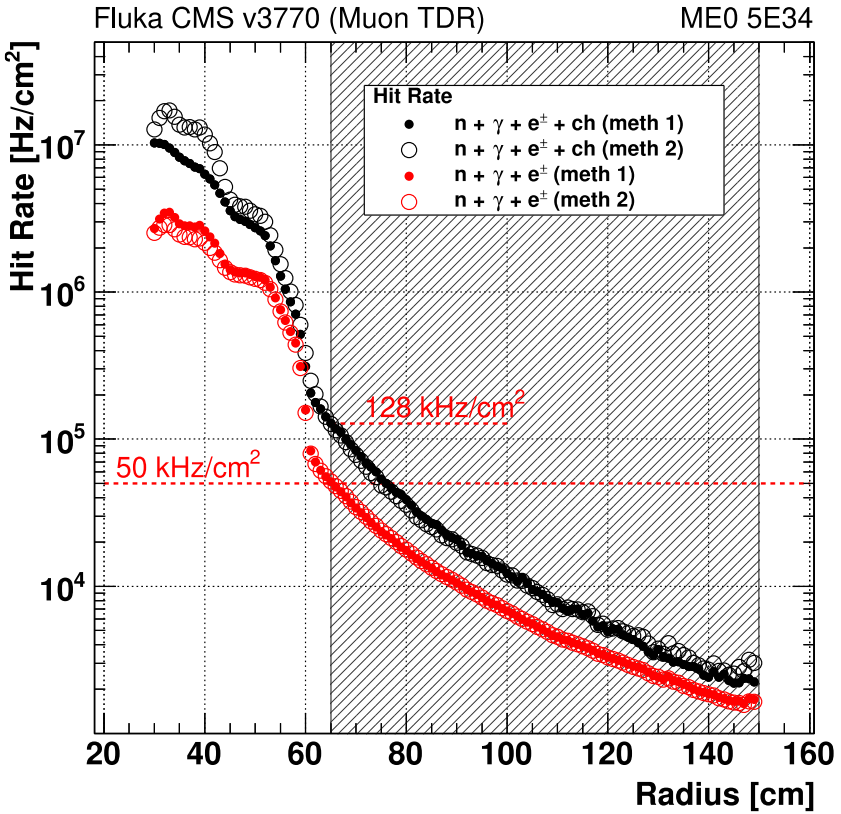
- In good shape to hit the target of having 8 fully operational production sites (compared to the 4 foreseen in the original schedule)

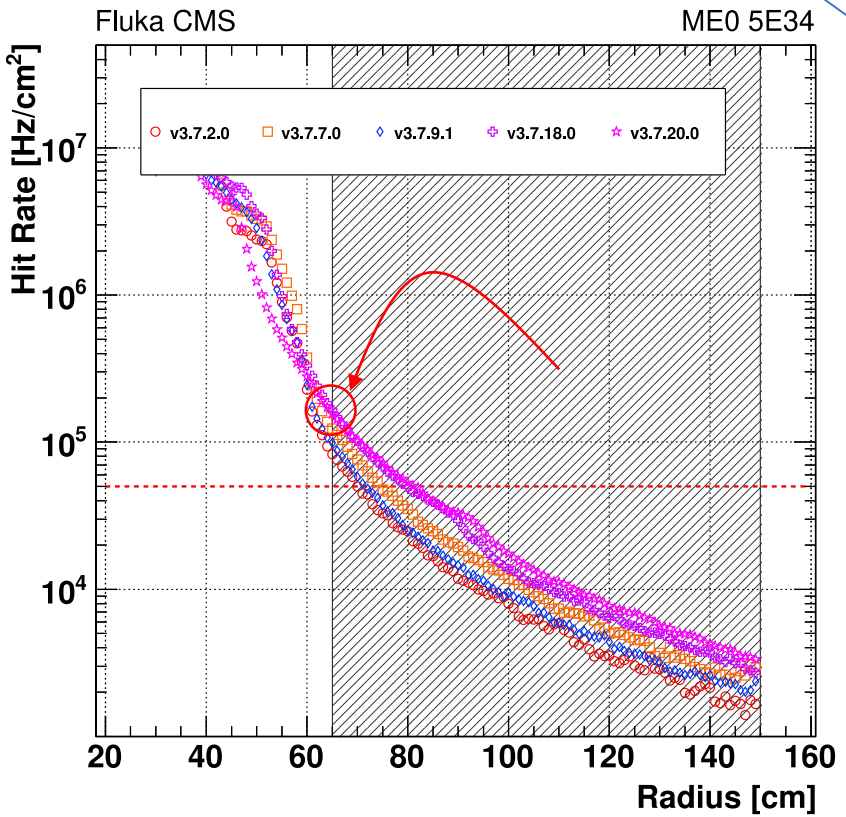
- All existing setups are available and operational

- New setups are on tracks to be fully operational when detector kits will be available
  - PU is investigating the possibility to obtain APV25 on-site
  - PKU has reached the last stage of the certification program

- Manpower situation is clear for both 2020 and 2021
  → Some teams will be partially renewed in 2021; need for additional training (see presentation on GE21 procurement)

Correction of Muon TDR hit rate





- **Left plot:** CMSSW 3.7.7.0 used for Muon TDR indeed predicts max 50kHz/cm^2 for ME0 (due to neutrons, photons & electrons)
  - **However additional 80 kHz to be expected due to protons (30kHz), pions (40kHz) & decay muons (10kHz)**
- **Right plot:** hit rate evolution starting with CMS Upgrade TP (v3.7.2.0) over Muon TDR (v3.7.7.0) and various implementations of HGCAL (v3.7.9-.1 v3.7.18.0-v3.7.20.0)
  - Old beampipe used in v3.7.2.0 (CMS TP) and v3.7.9.1 (HGCAL TDR)
  - New beampipe used in v3.7.7.0 (Muon TDR) and v3.7.18-20 (impl. of HGCAL TDR changes)

Effect of Double Shield at bottom and reduced Back Shield

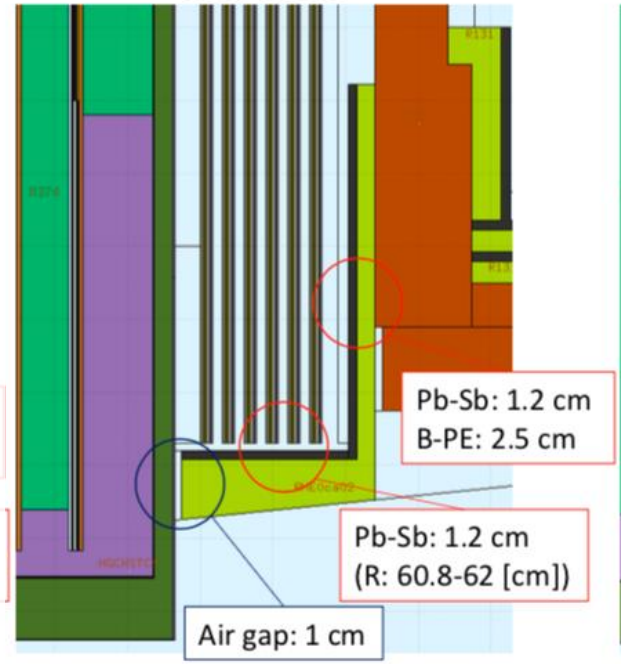
MEO

Baseline
v3.7.20.0*

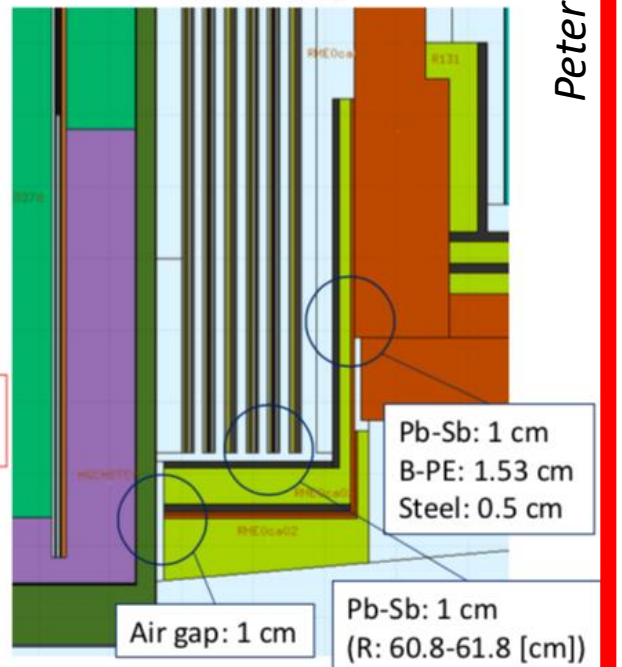
* https://indico.cern.ch/event/861694/contribu s/3639463/attachments/1943866/3224451/Radsim_phaseII_13112019.pdf

2/26/2020

Intermediate geo #1
v3.7.20.5



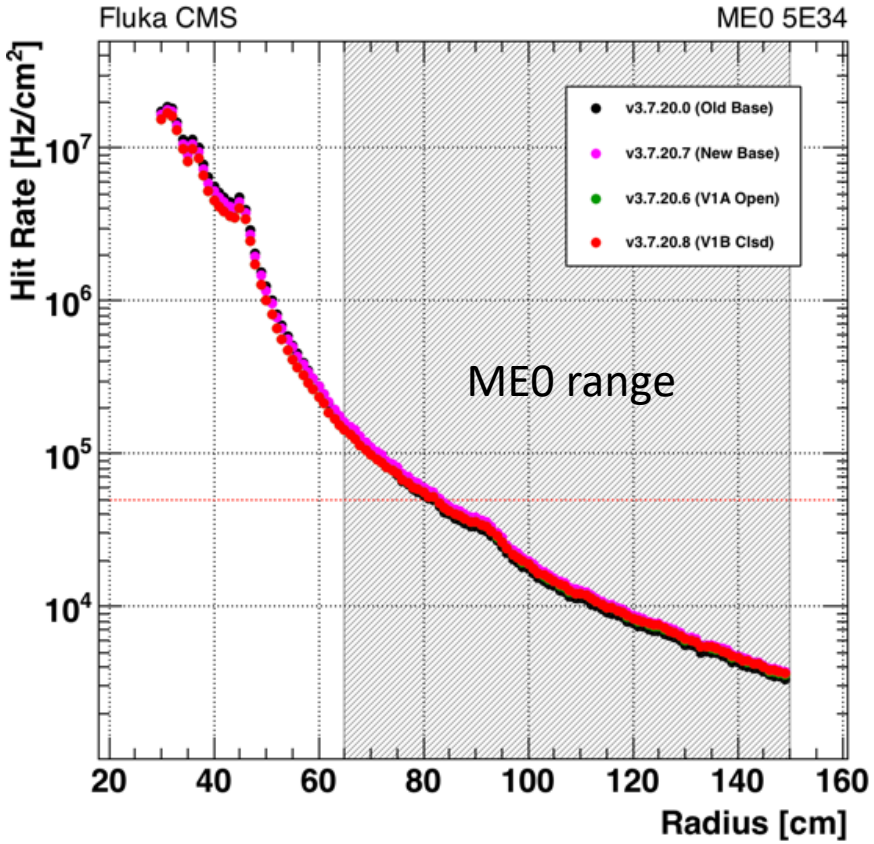
''Version 1B''
v3.7.20.6

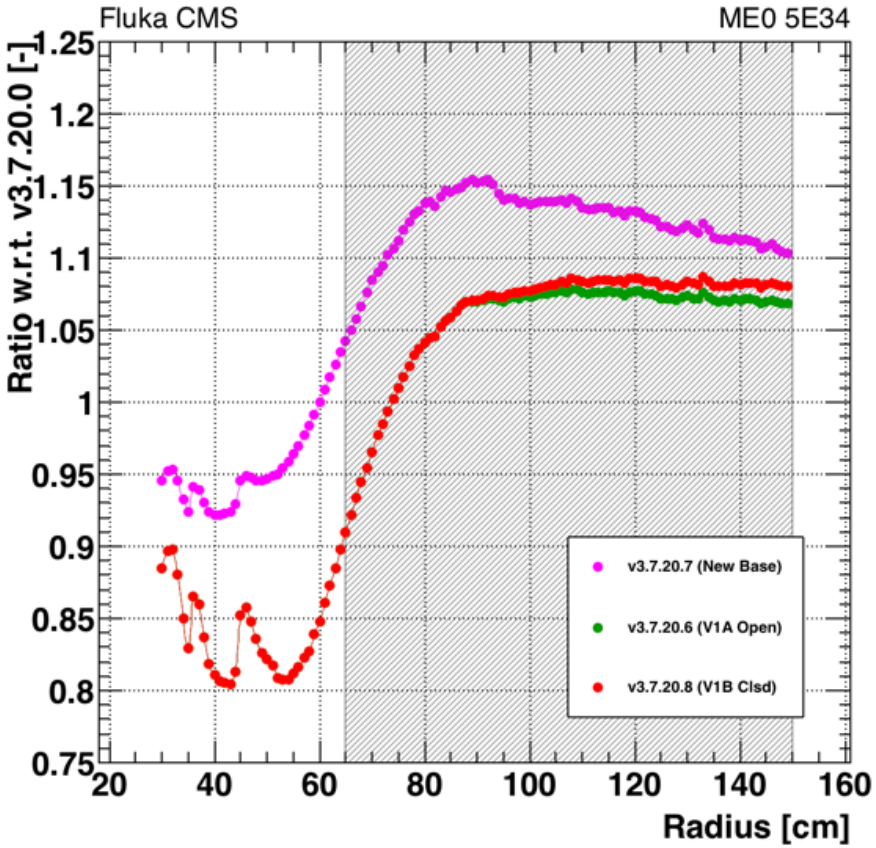


Peter Kicsiny

BRIL Radiation Simulation meeting 3

Combined Effect (New Baseline)





Piet Verwilligen

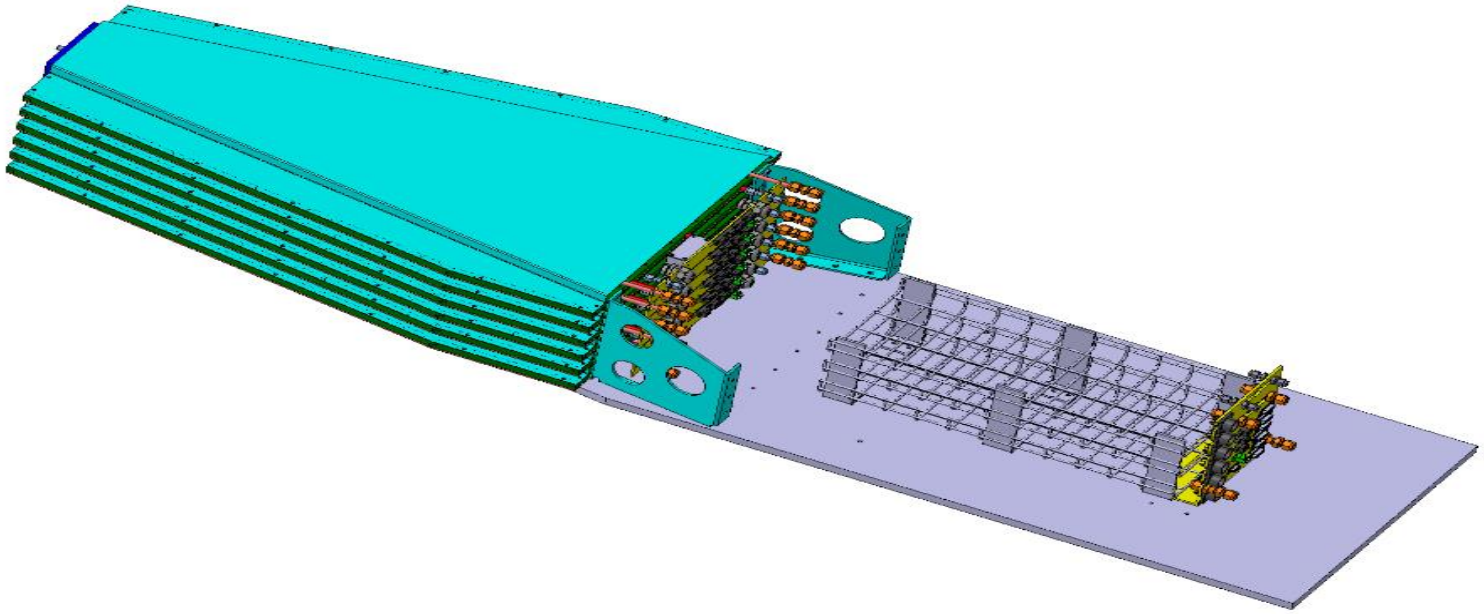
65 cm < R < 70 cm reduction of Hit Rate up to 10%
70 cm < R < 100 cm increase of Hit Rate up to 8%
R > 100 cm constant increase of Hit Rate with 8%

Old max: 155 kHz/cm^2
New max: 142 kHz/cm^2

ME0 Module preparation

- Module design completed in summer 2019, full design available in EDMS
- First two ME0 modules with double-segmented foils on all 3 GEM foils assembled by end 2019 in CERN
- Two ME0 kits shipped to FIT, one module fully assembled, first largely used for X-talk studies
- Three similar additional kits shipped to Bari right before lockdown, waiting for assembly; clean room compatibility with COVID-19 prescription to be verified
- Two kits at CERN, waiting for 904 clean room availability

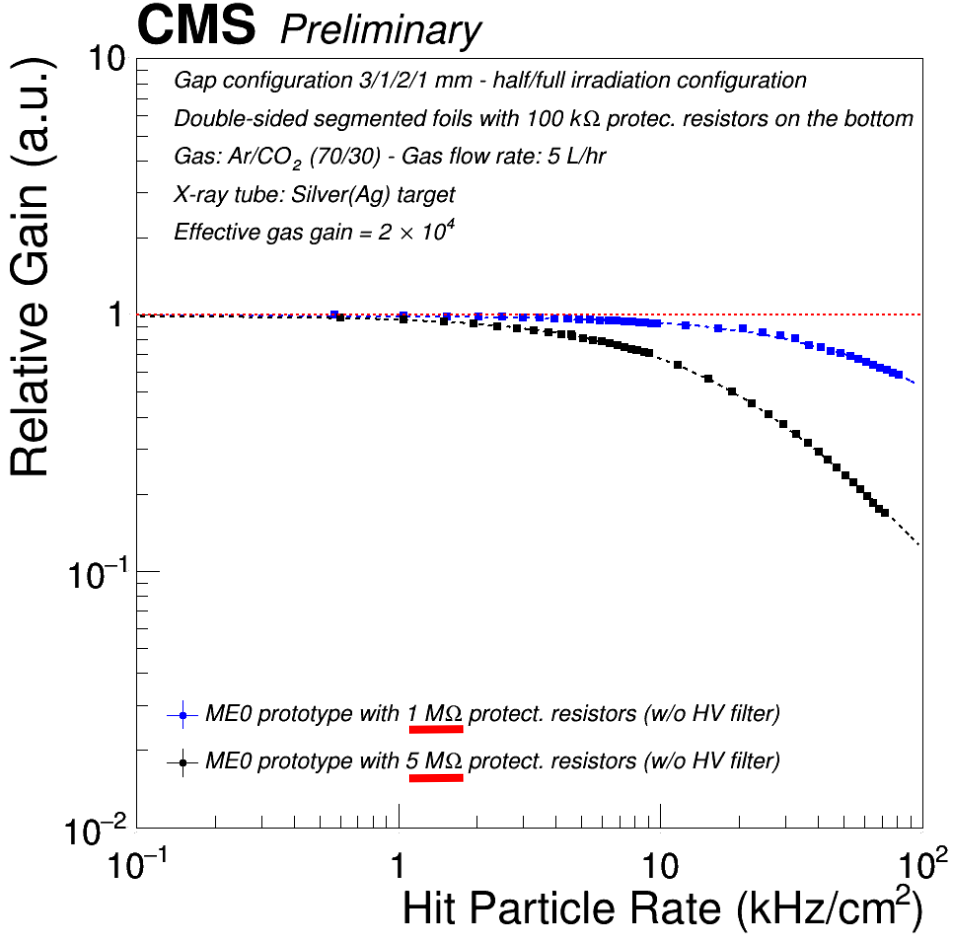
ME0 Stack design Status



- **Procurement of mechanical components for first ME0 stack ongoing with the help of Barthel Philipps (Aachen); components are expected at CERN at latest in Sept 2020, in time with arrival of ME0 modules to be assembled in Bari**
- Stiffeners will be prepared both for Face-Up and Face-Down Stack types, this will allow to perform mechanical test of both Stack types

Rate capability studies on ME0 prototype

Comparison between the ME0 module with **1 *MΩ protect. resistors (w/o HV filter)*** and ME0 module with **5 *MΩ protect. resistors. (w/o HV filter)***



1) the ***protection resistors*** on the GEM-foils are used ***to quench*** the ***self-sustained discharge***
2) obviously the ***best protection*** is obtained with ***very high value resistors*** $O(10M\Omega)$

but on the other hand ...

3) the ***experimental requirements*** (particle rate and gas gain) determine the ***maximum values*** that can be used to maintain the potential drops within acceptable limits under high-flux irradiation
4) the ***power supply system*** (i.e. its max. output current) determine the ***minimum values*** that can be used to maintain the total current below the limit of the HV board (***even in case of possible short-circuit in the HV sector***)

The bkg. rate, discharge phenomena, rate capability, power supply limit and HV sector area must be taken into account to choose the protect. resistor value

Rate capability studies on ME0 prototype

The rate capability of the ME0 prototype with ***1 MΩ protection resistors*** was measured in Ar/CO_2 $(70/30)$ at gas gain of 2×10^4

1) The rate measurement was performed in ***current mode*** due to the high particle flux (see slide 7)
2) Three different configuration was tested:
   → ***blue dots***: with standard HV filter + 100% of the area is uniformly irradiated

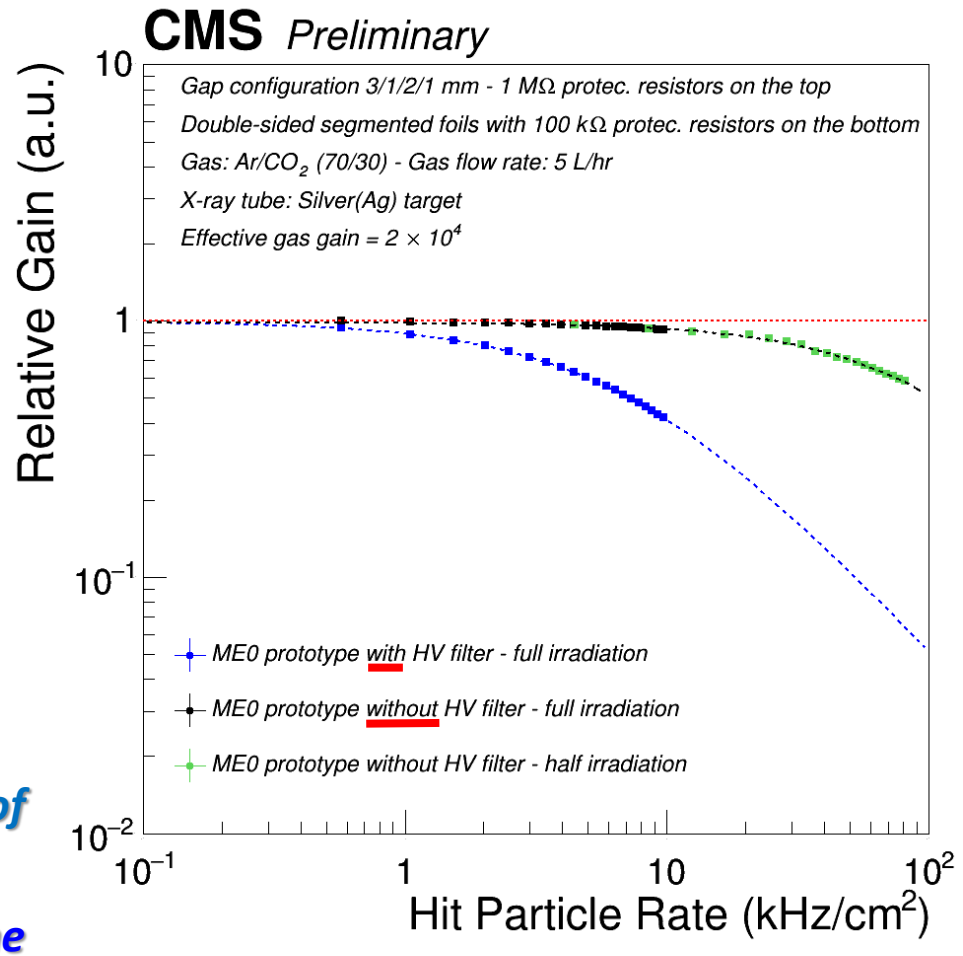
   gas gain drop of 30% @ $3\ kHz/cm^2$

   → ***black dots***: without standard HV filter + 100% of the area is uniformly irradiated

   → ***green dots***: without standard HV filter + 50% of the area is irradiated

   gas gain drop of 30% @ $50\ kHz/cm^2$

- ***the stringent ME0 requirements in terms of rate capability are not fulfilled*** ***(see Piet's talk)***
- ***the HV filter has a significant impact on the detector rate capability!***

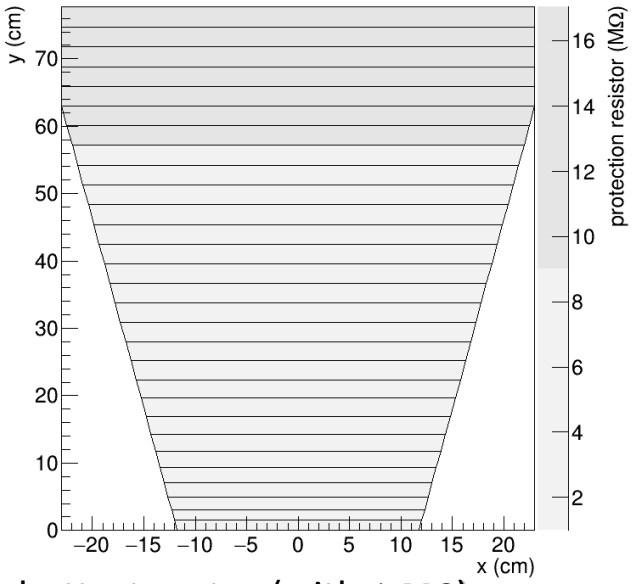


N.B.: Current Best estimate for max. rate in ME0 is 142 kHz/cm^2

Novel double-sided segmented foil design

3rd configuration-V_1: old double-sided segmented foil design with ***different-area HV sectors*** and ***different-value protect. resistors***

1 MΩ (lowest) protect. resistors

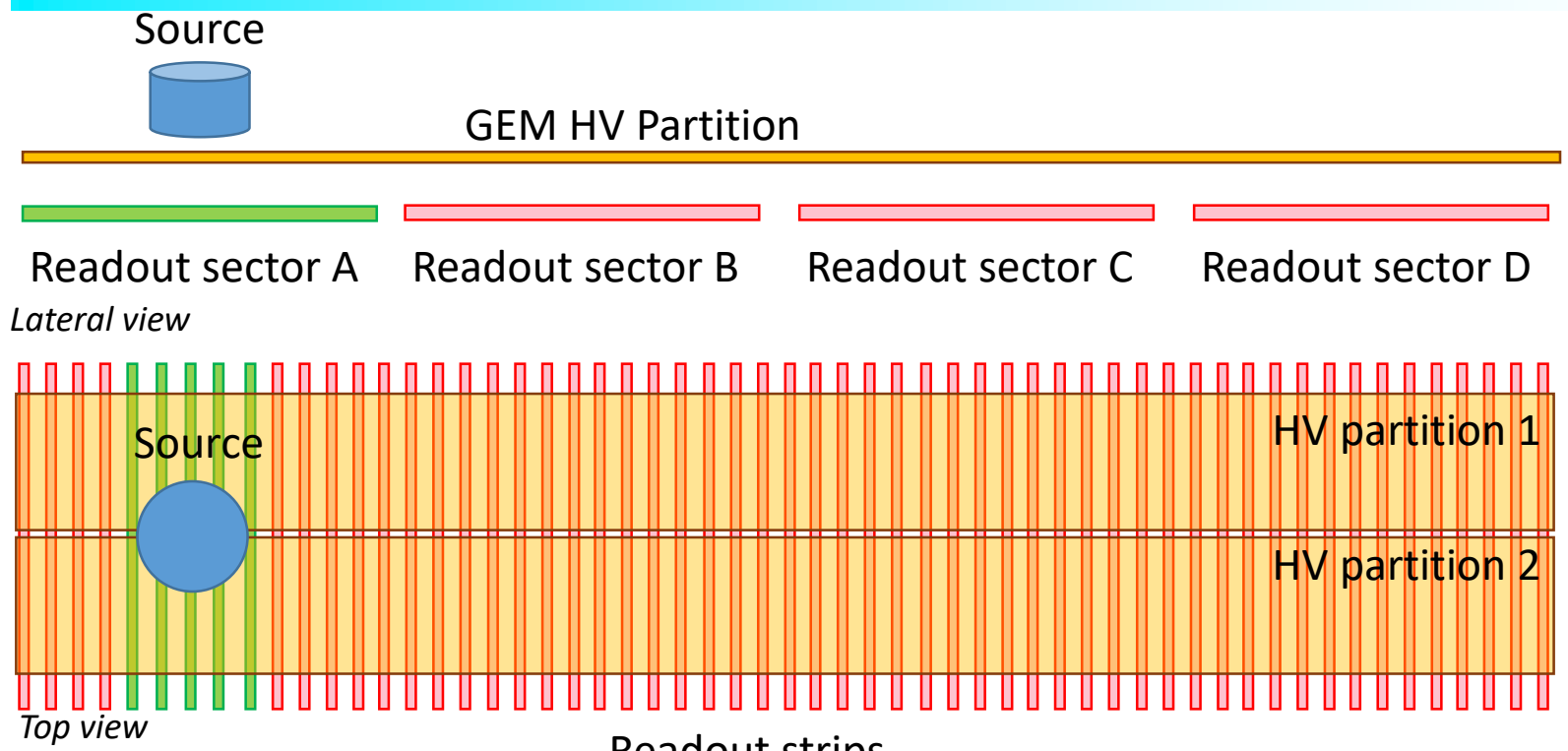


- expected curret in hottest sector (with $1\ M\Omega$):
  $5.3\ \mu A/sector$
- expected curret in coldest sector (with $17\ M\Omega$):
  $0.3\ \mu A/sector$
- expected voltage drop:
  $5.3\ V/sector$
- max number of tolerable shorted segments: $1\ per\ HV$ ch.
  (estimated for the lowest protect. resistor values)

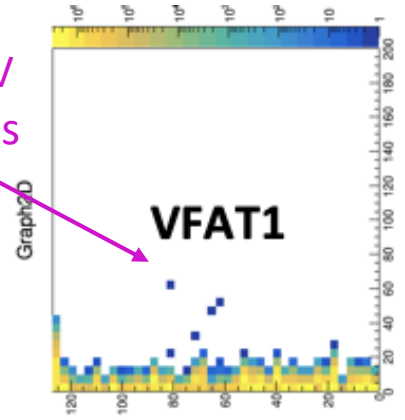
coldest areas → *hottest areas*

R/O SECTOR	HV SECTOR	AREA SECTOR (cm^2)	PROTEC. RESISTOR ($M\Omega$)	
$\eta = 1$	1	186.76	17.05	
$\eta = 1$	2	323.35	16.12	15 MΩ
$\eta = 1$	3	459.94	13.4	
$\eta = 1$	4	593.90	13.52	
$\eta = 1, 2$	5	727.86	12.66	
$\eta = 2$	6	132.57	11.82	10 MΩ
$\eta = 2$	7	129.77	10.11	
$\eta = 2$	8	126.91	8.62	
$\eta = 2, 3$	9	123.99	8.95	8 MΩ
$\eta = 3$	10	120.99	7.97	
$\eta = 3$	11	117.92	6.94	
$\eta = 3$	12	114.77	5.63	
$\eta = 3, 4$	13	111.53	5.87	5 MΩ
$\eta = 4$	14	108.19	5.06	
$\eta = 4$	15	104.75	4.56	
$\eta = 4, 5$	16	101.19	3.51	
$\eta = 5$	17	97.50	3.67	3 MΩ
$\eta = 5$	18	93.67	3.30	
$\eta = 5, 6$	18	89.67	2.44	
$\eta = 6$	20	85.49	2.44	2 MΩ
$\eta = 6$	21	81.10	2.22	
$\eta = 6$	22	76.45	1.76	
$\eta = 6, 7$	23	71.51	1.44	
$\eta = 7$	24	66.20	1.47	
$\eta = 7$	25	60.42	1.26	
$\eta = 7, 8$	26	54.04	0.98	1 MΩ
$\eta = 8$	27	46.79	1.08	
$\eta = 8$	28	38.20	1.12	
$\eta = 8$	29	35.70	1.00	

Cross-talk Signals

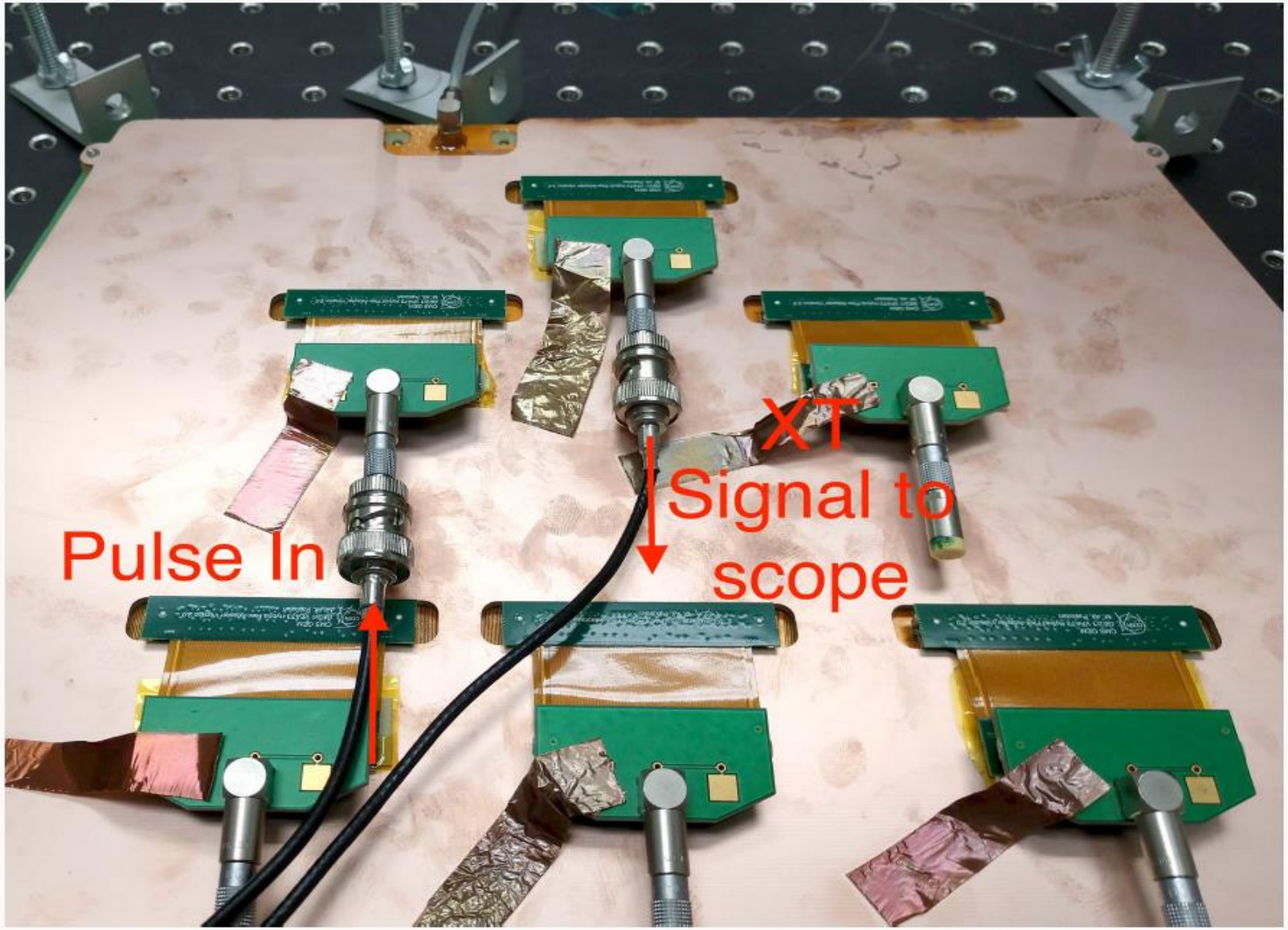


Other HV partitions are not affected

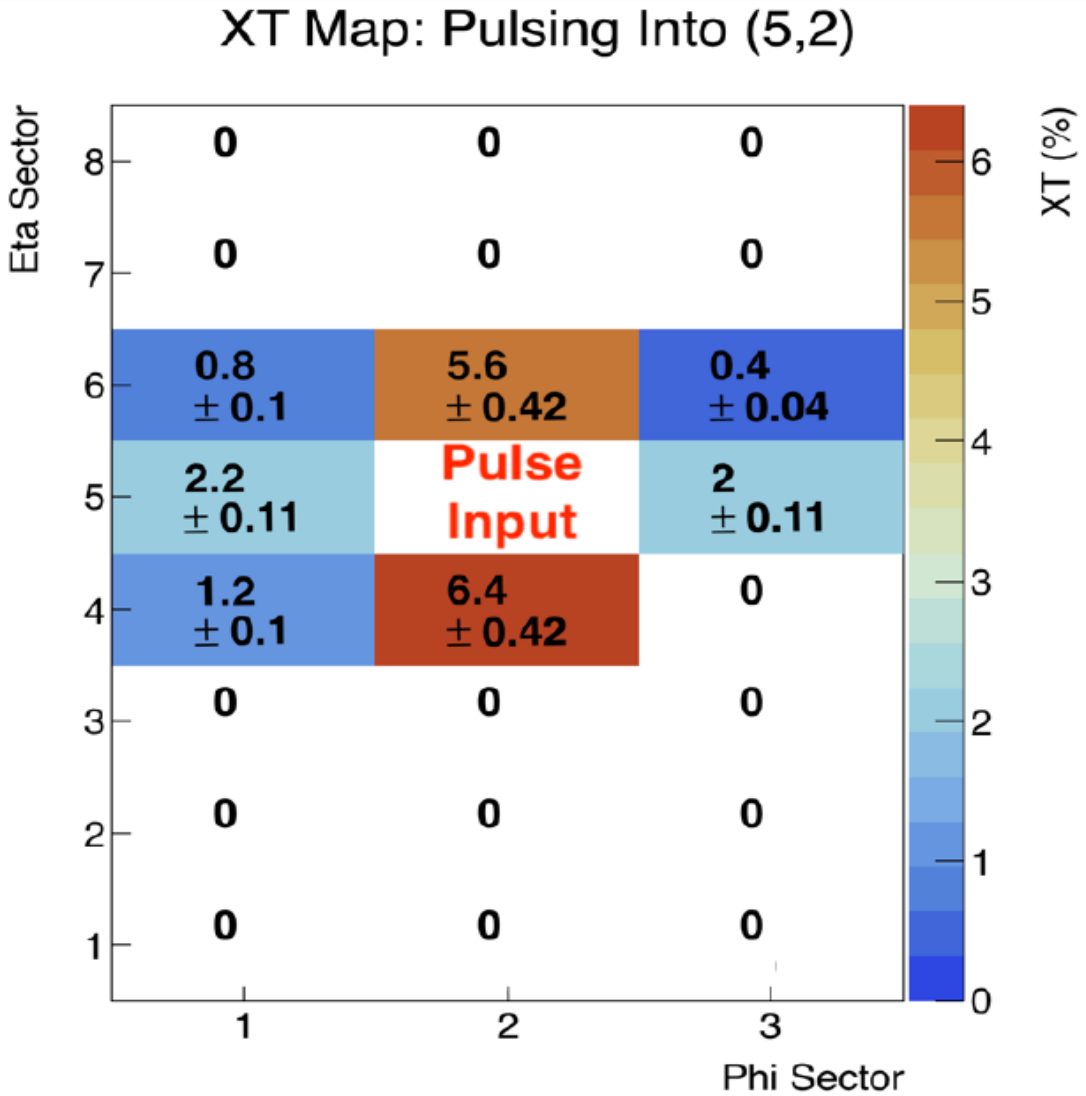


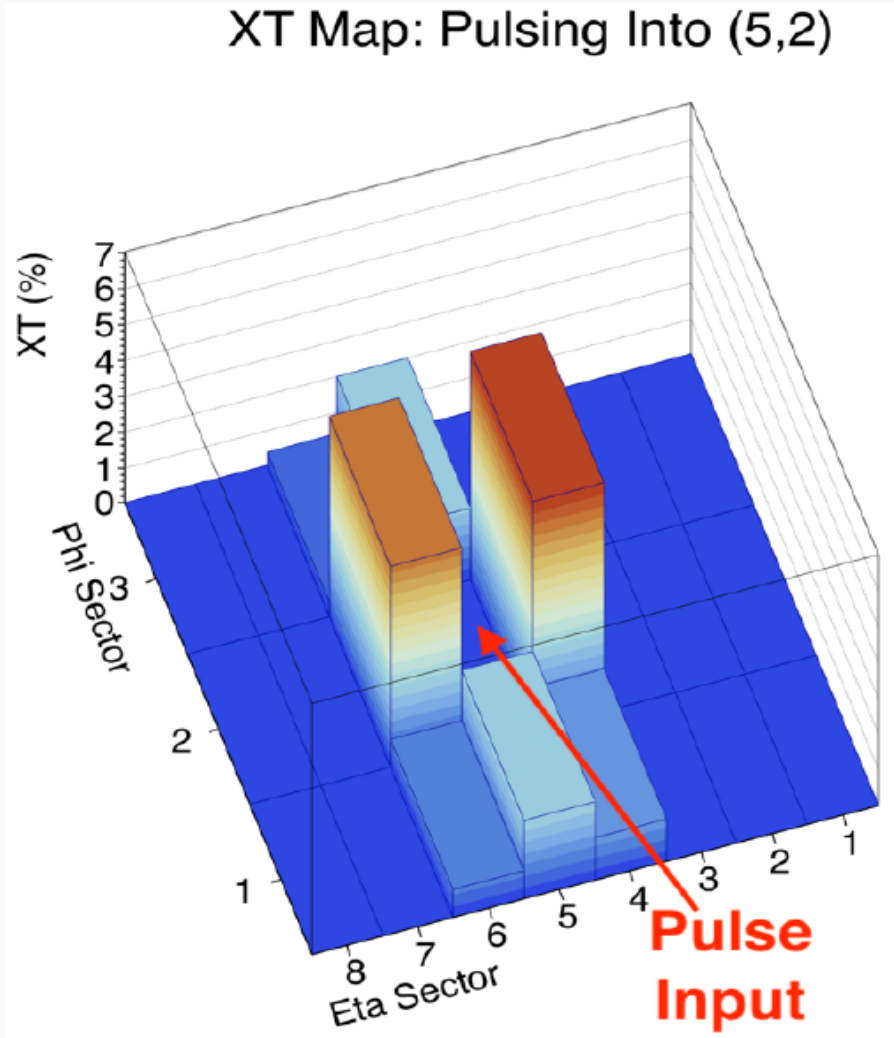
Experimental Setup at FIT

Pulsing into a readout sector and reading out of a readout sector:



XT Map: Pulsing into (5,2)

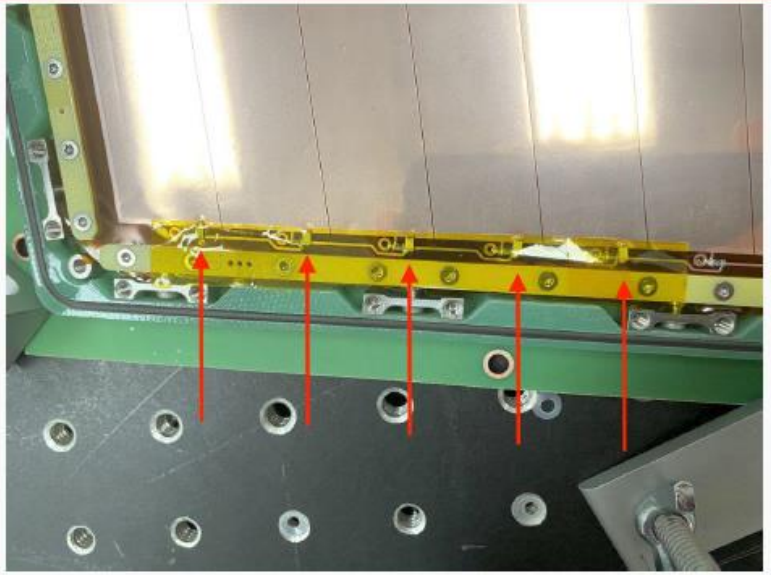




Modifying GEM3B

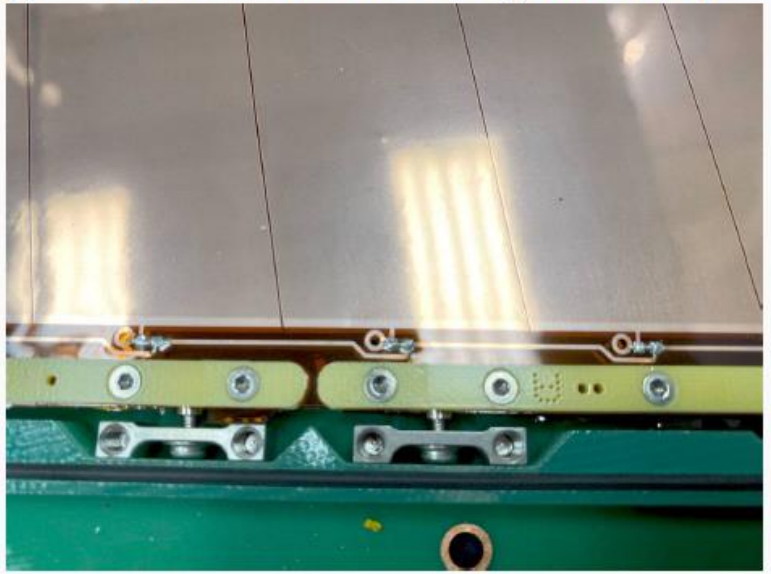
Mitigation Strategies

- The following modifications made to GEM3B:
  - 5 330±5% pF bypass capacitors (`https://www.digikey.com/product-detail/en/yageo/CC1206JRNP0BBN331/311-4435-1-ND/8025524`) were soldered to the the HV segments on GEM3B in $i\eta = 8$ and covered with Kapton tape (without the Kapton tape, there was a short between GEM3B and the $i\eta = 6 - 8$ RO sectors)
  - Three protection resistors on the HV segments in $i\eta = 5$ on GEM3B were removed and connected together with solder
- Square pulse with 500 mV amplitude and 1 μs width was used for all XT maps [except for the baseline configuration in (5,1)]
- We will present the "unmodified" baseline XT map, the modified XT map, and a map that shows the change in XT for 6 RO sectors



Bypass capacitors on the HV segments in $i\eta = 8$

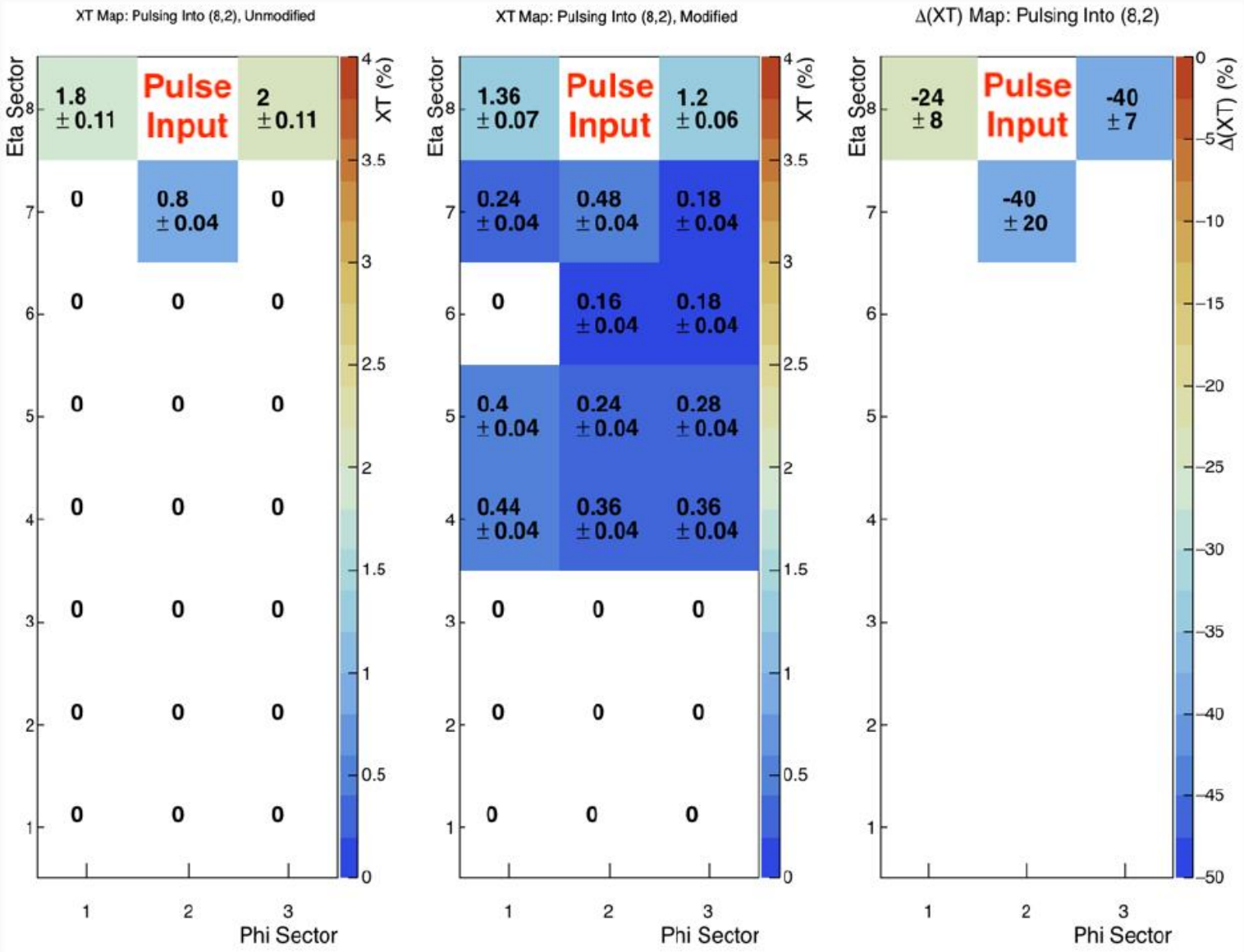
1) Add bypass capacitors to prot. resistors



HV segments in $i\eta = 5$ connected together

2) Increase segment size

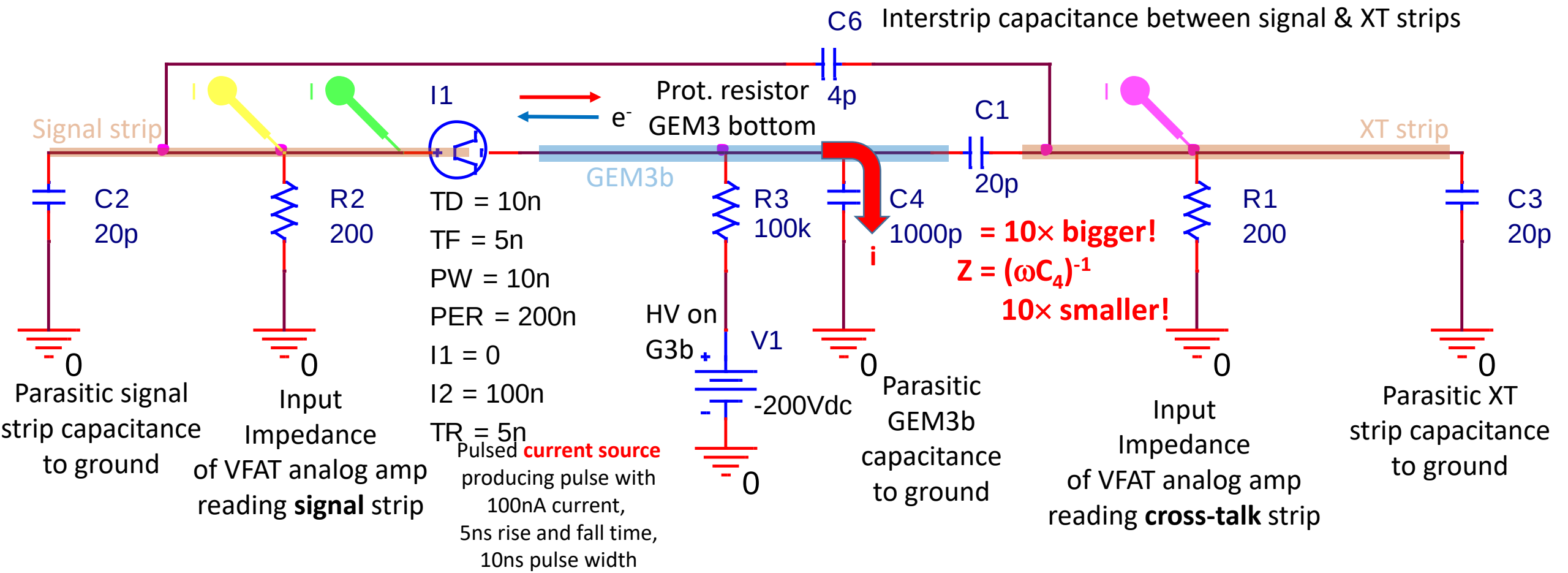
XT Maps: Pulsing into (8,2)



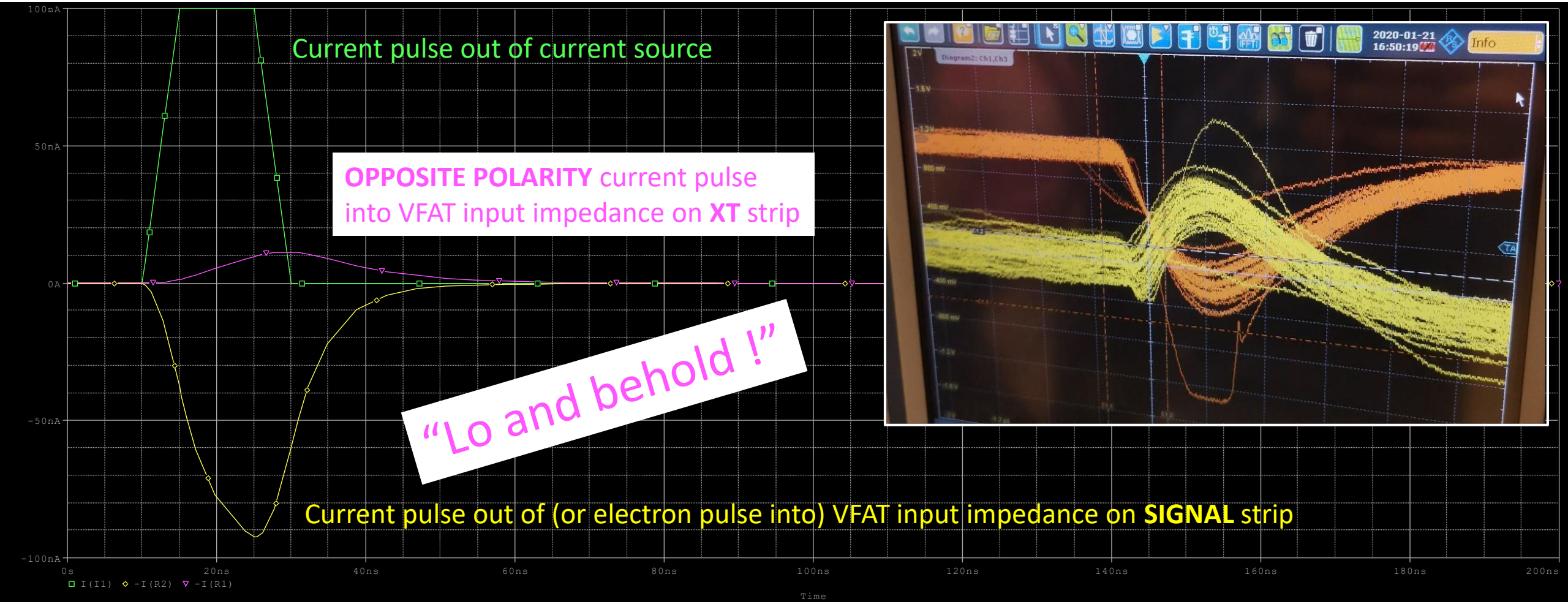
Crosstalk reduced

Increased GEM3b capacitance to GRD

- In this circuit, the increased capacitance of GEM3 bottom provides a **much reduced impedance Z for sinking the current from the current source to ground.**
- As a consequence, the amount of XT current that can flow into C1 is reduced.
- **This explains why XT is observed on double-segmented foils, but not on single-segmented foils!**

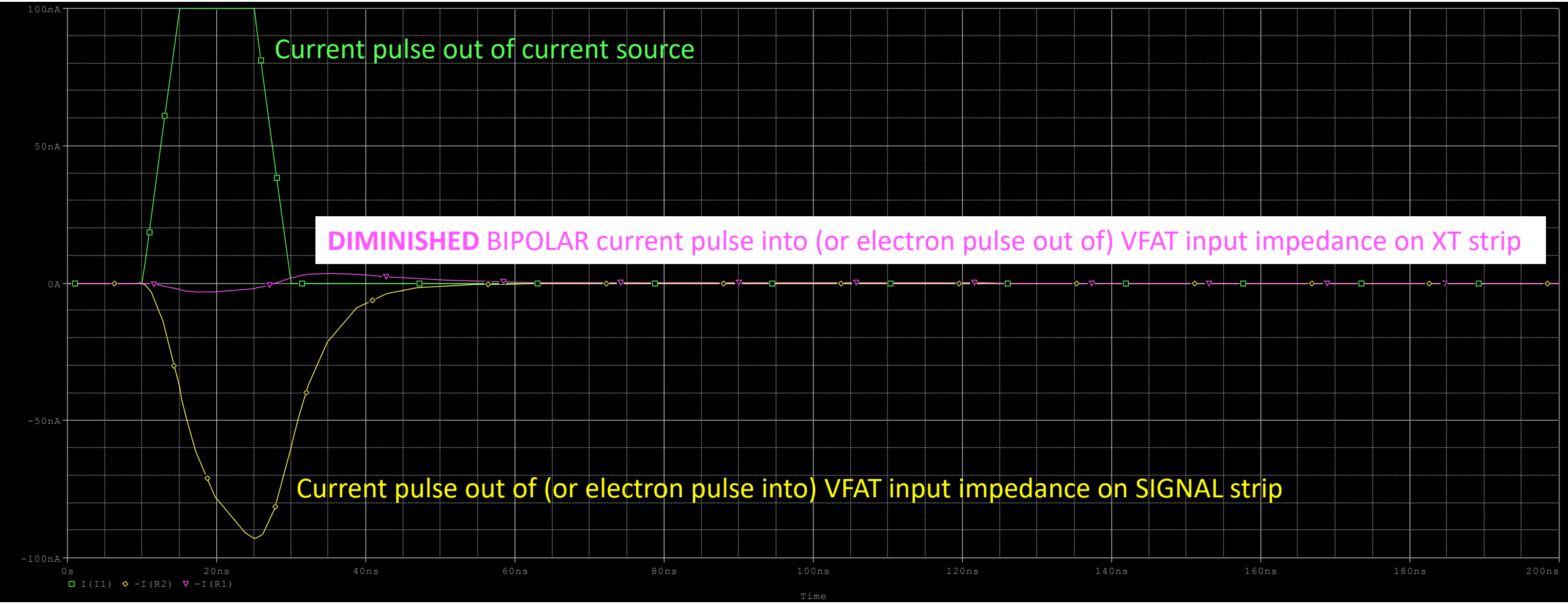


Pulse analysis for gas avalanche mode



Main observation: The electron pulse into the VFAT amp connected to the **signal strip** (yellow) and the electron pulse into the VFAT amp connected to the **XT strip** (purple) now have **OPPOSITE polarity!** This is different from the result with the pulser where we have same polarity.

Increased GEM3b capacitance to GRD



Main observation: The XT pulse is DIMINISHED by a factor ≈ 4 and becomes bipolar!

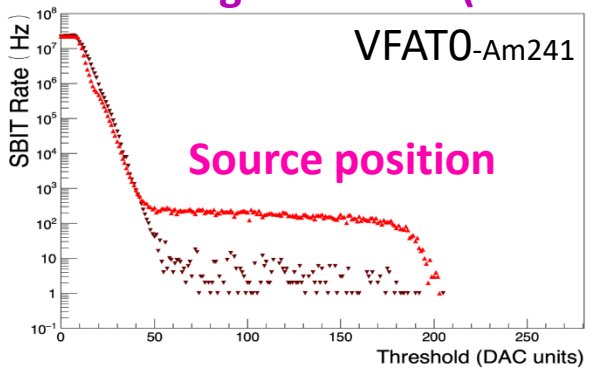
SPICE Model - Summary & Conclusions

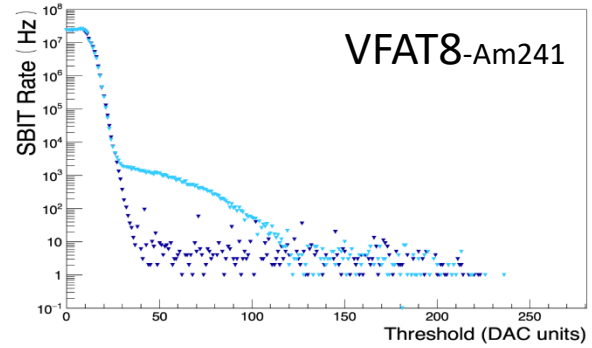
Results from the PSPICE model of the GEM crosstalk circuit

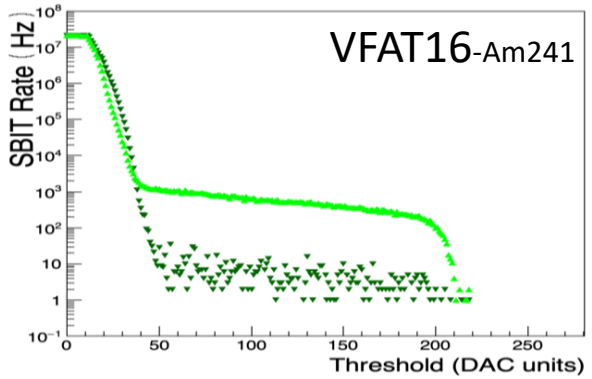
- replicate experimental XT results obtained with a voltage pulser at FIT
- explain why tests with a voltage pulser produce *same-sign* XT pulses while tests with a GEM in normal operation produce *opposite-sign* XT pulses as due to the difference between an external voltage source and an internal current source
- show that any method for reducing the *impedance Z of GEM3-b to ground* will reduce XT:
  - GEM3b foil segments with larger capacitance ($Z = 1/\omega C$)
  - connection of GEM3b foil without protection resistor (as in GE1/1)
  - bypass capacitor on 100kΩ protection resistor
- show that this mitigation has no significant impact on signal integrity
- show that additional devices upstream of a large protection resistor will be ineffective
- caution that the mitigation of this "GEM3-bottom to ground impedance" has its limits due to the additionally present impedance from the interstrip capacitance
- show that XT can be expected to be reduced by up to a factor ≈ 4 by this type of mitigation
- show that by reducing the protection and HV filter resistances, the GEM3-bottom to ground impedance XT and the interstrip capacitance XT can cancel each other and net XT becomes zero
- demonstrate a need for careful balancing of discharge mitigation and XT mitigation

Hardware Test

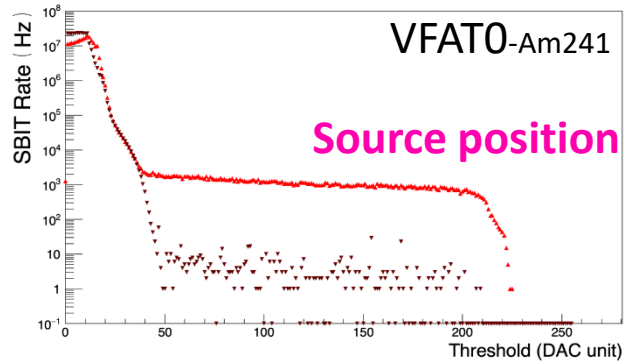
Fine HV segmentation (100cm^2)

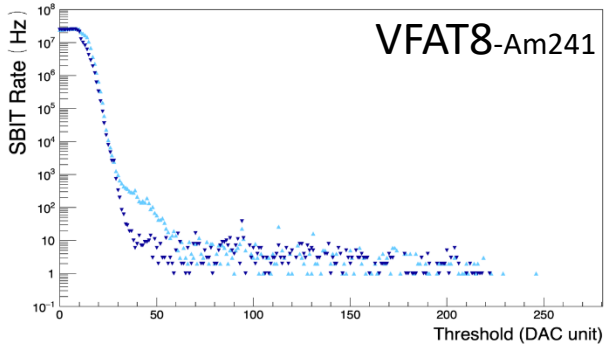


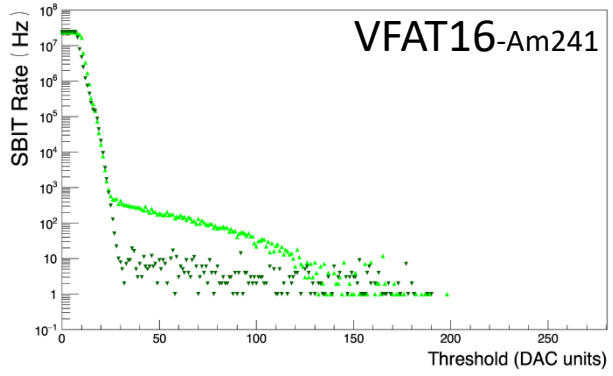




Large HV segmentation (1000cm^2)



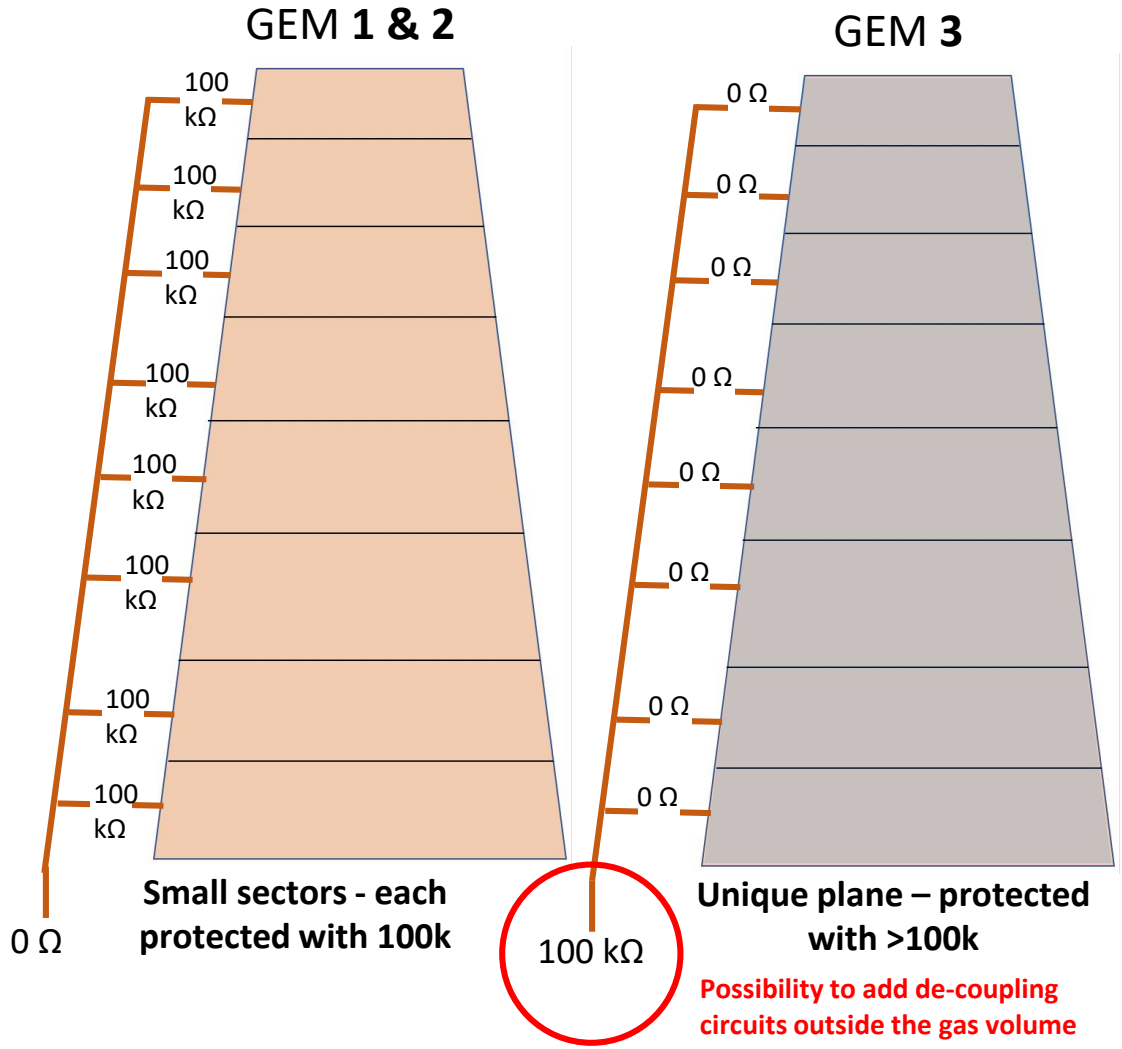




- → Same studies performed on small and large HV segmentation
- → X-talk is reduced, but still present and measurable with larger HV segments
- → X-talk probability is reduced by a factor >3 when increasing the HV segment size by a factor 10
- → X-talk amplitude is also small with large HV segments (i.e. lower dead time)

Remaining R&D

Same layout (i.e. production mask) for all three foils
Minor modifications with respect to current design



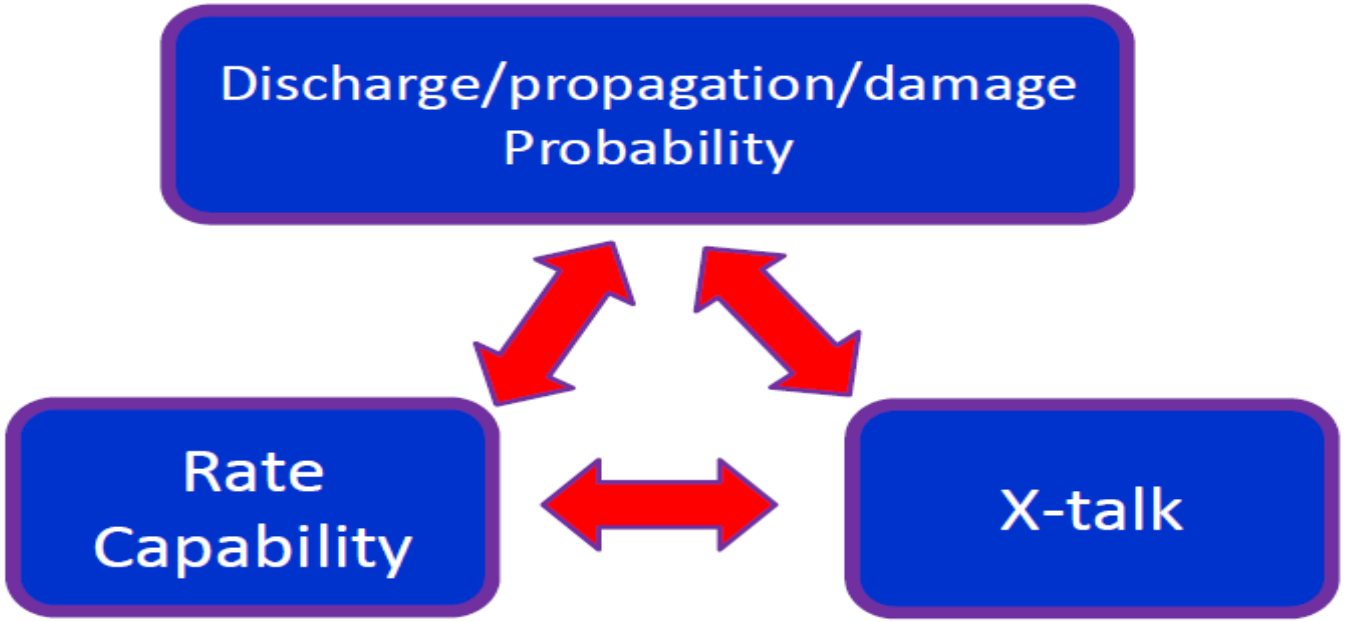
→ Promising option to cope with X-talk and maintain the current design
→ No need to re-make new masks

However, moving back to large induction capacitance may bring back the discharge propagation issues:

- Necessary to test this configuration with large detectors to confirm the X-talk probability and quantify the impact on the discharge behavior

Time line:
- T0 is set whenever a prototype is ready and operational. At CERN, T0 is just after the R&D is possible in the 904 lab and a clean room is available (exp. mid of June). In FIT, T0 is when the ME0 prototype is fixed and re-assembled (exp. beginning of June)
- T1 = T0 + 2 weeks discharge tests completed
- T2 = T1 + 2 weeks X-talk tests completed, ready for final discussion

Future for ME0 project



- We have a lot of options for ME0 and room for improvement
- By the way, every change in the foil segmentation, HV scheme … Has to be checked for both the 3 effects

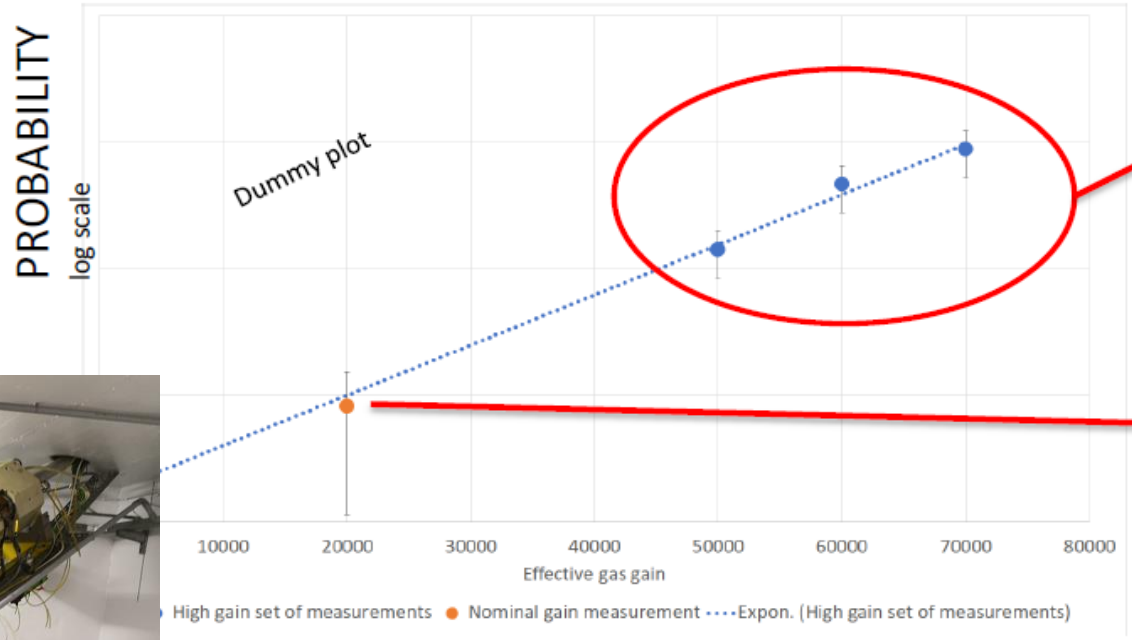
- In ME0 case, the number of discharges will be very high: it will be necessary to test the realibility of the detector perfomance under a high number of discharges (an «aging» test from the discharge point of view) - 10x10 GEM will be enough –
- Designing a tool for discharge monitor during CMS operation (using the knowledge gained during these R&D years)

Measurements plan

Next neutron test

Louvain neutron facility:
Up to 3 × 10^8 n/cm^{2}s

Measure DISCHARGE, PROPAGATION and DAMAGE probabilty with a neutron beam



High gain, high discharge rate measurements (at least 3 points for an exponential fit)
2 hour each point

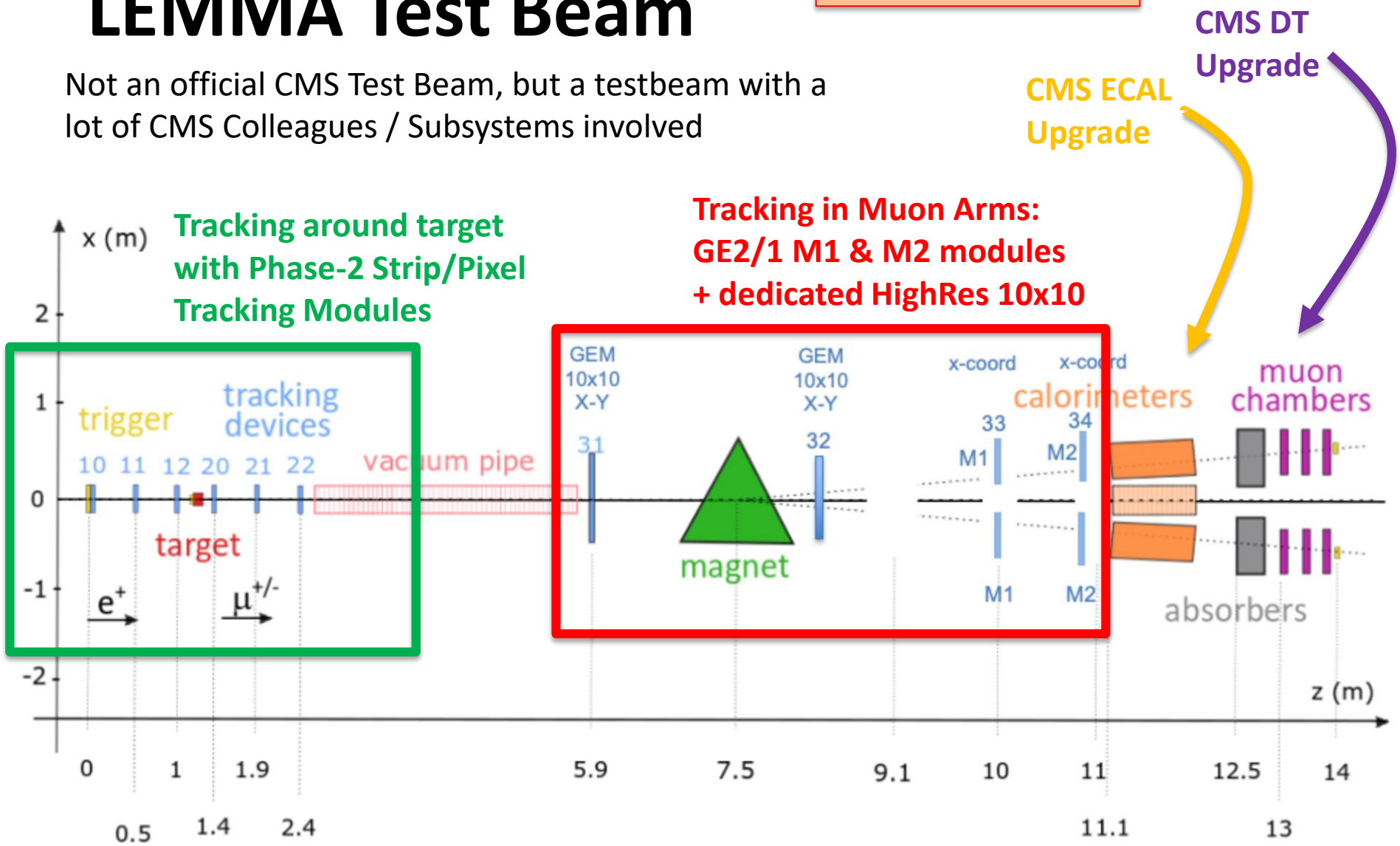
Nominal gain, «low» discharge rate measurements
6 hour

Cross check the low statistics measurement at nominal gain

Proposal for 2021 LEMMA Test Beam

All read by final CMS DAQ (Phase 2)

Not an official CMS Test Beam, but a testbeam with a lot of CMS Colleagues / Subsystems involved



Electronics & DAQ

GE2/1 electronics status	*Dayong Wang*	
CERN	09:30 - 09:55	
ME0 electronics status	*David Saltzberg*	
CERN	10:00 - 10:25	
Backend DAQ status	*Evaldas Juska*	
CERN	10:30 - 10:55	
Interstrip capacitance sim. & measurement	*Dr Shivali Malhotra et al.*	
CERN	11:00 - 11:25	
Status test stands & measurements; future measurements	*Mykhailo Dalchenko*	
CERN	11:30 - 11:55	
Plans for ASIC testing	*Gilles De Lentdecker*	
CERN	12:00 - 12:25	
General discussion		
CERN	12:30 - 13:00	

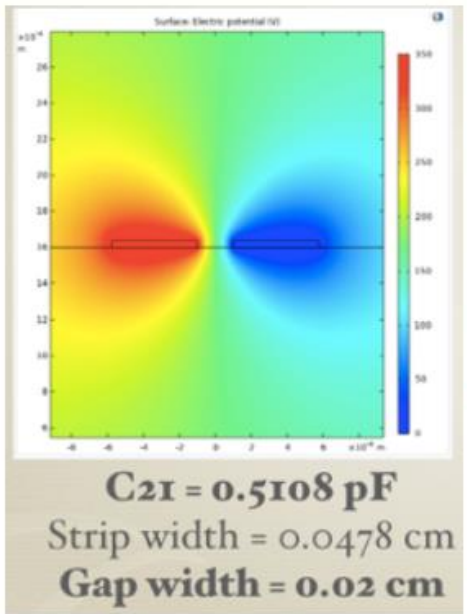
Interstrip capacitance on GEM Readout Board

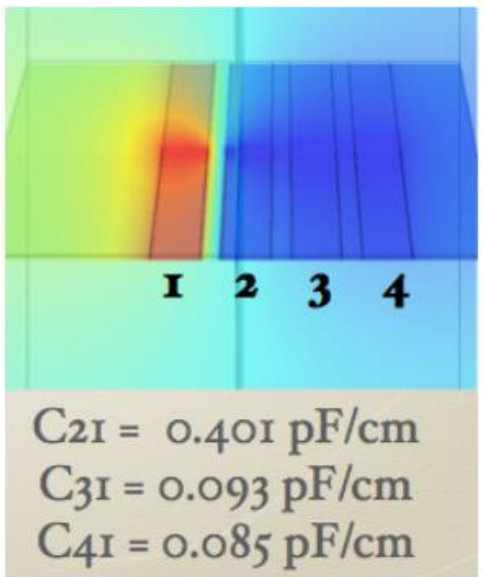
- Analytical calculation
- Finite Element Analysis
- Direct measurements

(Pub. in preparation)

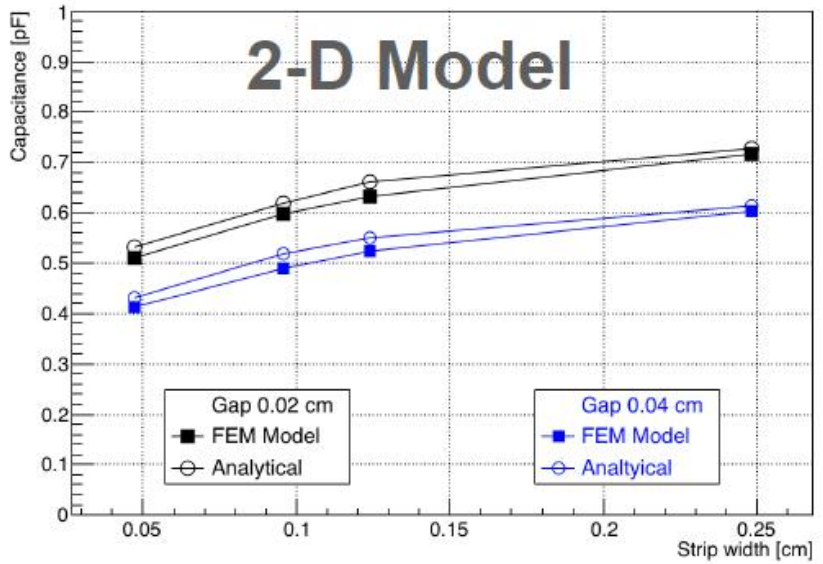
FEA for GE2/1 using COMSOL

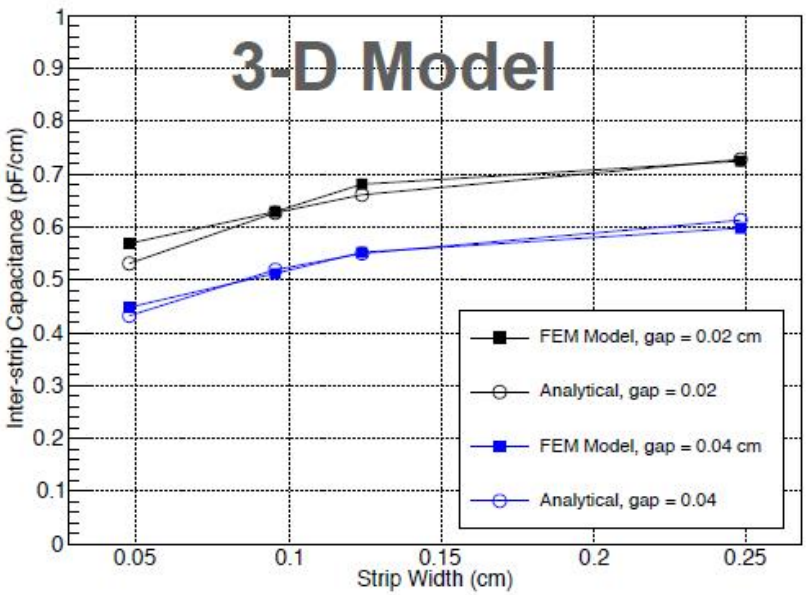
- Used MATLAB for two strips
- Now using COMSOL for multi-strips
- Compared results for M1 & M4 size strips with analytical calculations (CMS IN-2018/006)
- Extended 2-D model to 3-D with multi-strips using COMSOL





9

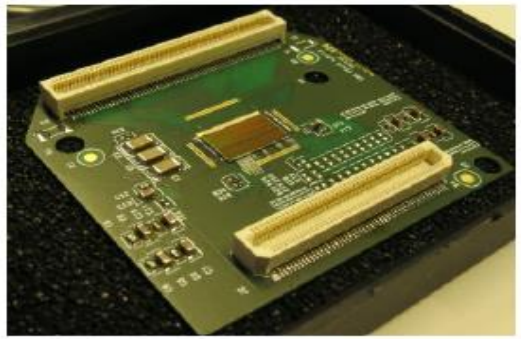




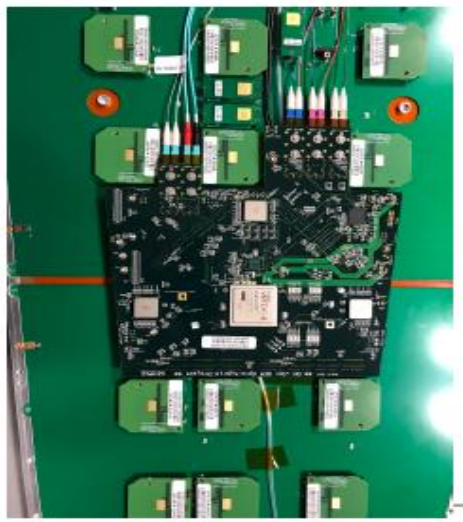
Lessons learned from GE1/1

- **Substantial design modifications relative to the conceptual (TDR) design**
  - **A number of them driven by the GE1/1 experiences**

➢ In GE1/1, VFAT3 die bonded on hybrid:

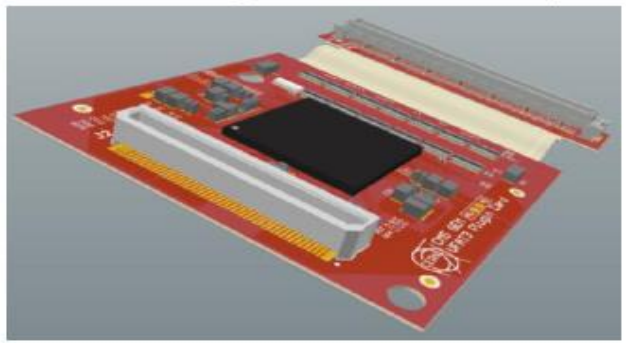


GE1/1 hybrid:
- VFAT3 dies assembled on a small (~4.5 x 4.5 cm² rigid PCB)
- PCB difficult to manufacture and to bond, because of the small bond pitch (60 um)

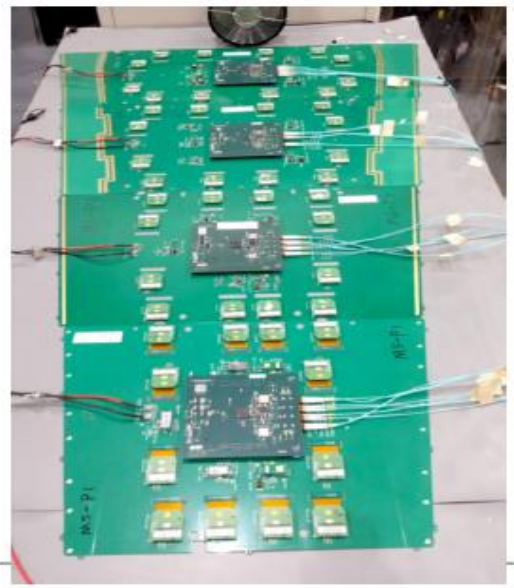


GE1/1:
- Optohybrid connected to two independent GEB half-boards
- Increased potential for mechanical stress
- Evolved powering schema and grounding

➢ In GE2/1, a packaged VFAT3 on a Rigid+Flex PCB (PlugIn card):



The flex part absorbs residual misalignment of GEB vs ROB
- Rigid part is also hosting VFAT3 input protection circuit



GE2/1:
- Each module has its own OH
- No potential for mechanical stresses from misalignments
- Independent powering, separate grounds
- Small lower power FPGA (Artix-7)

VFAT3 packaging status

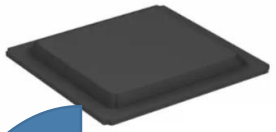
Deliverable/milestone	Relative timescale	Estimated/actual date
Placement of the order by CERN	T_0	Half July 2019
Design files and associated reports	T_1	October 2019
Approval by CERN of the substrate design	T_2	October 2019
Delivery of the prototypes	T_2 + 8 weeks	December 2019
Approval by CERN of the prototypes	T_3	June 2020
Approval by CERN to start work on the series production	T_4	June 2020
Delivery of the series production (first batch)	T_4 + 4 weeks	July 2020

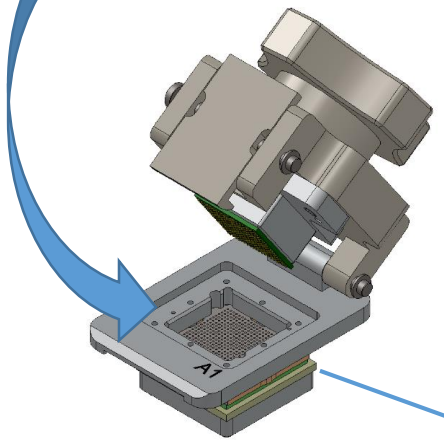
200 pc

- It took some time for ASE got the remain component (high precision resistor for current monitoring).
- The substrate mounting(just passive components). Some scratches on wafer, should be OK
- VFAT3 placement, bonding and encapsulation.
- VFAT3 should arrive at CERN around 26th May.
- **Latest update: the 200 packaged VFAT3 prototypes have been shipped out to IMEC. they will be shipped to CERN soon**
- the packaging test hardware ready, FPGA firmware OK, sw in development

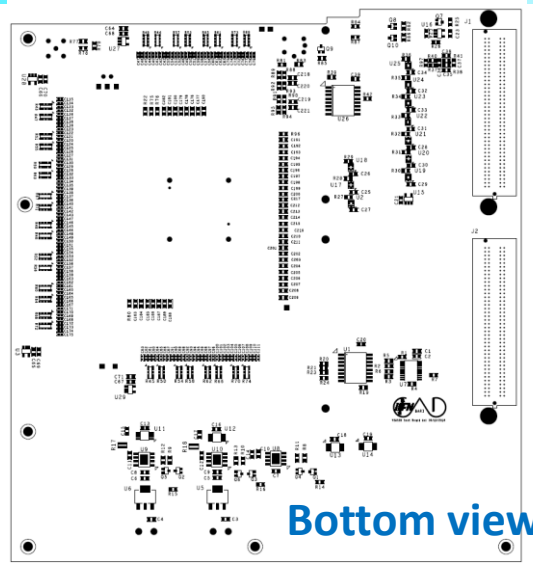
Setup to test packaged VFAT3

Packaged VFAT3

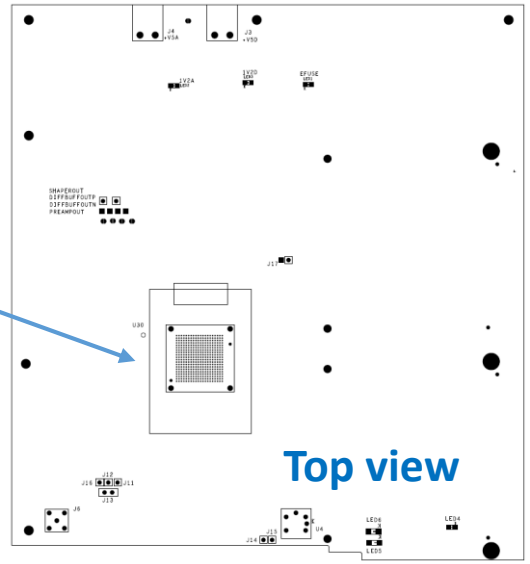




Clam shell socket



Bottom view

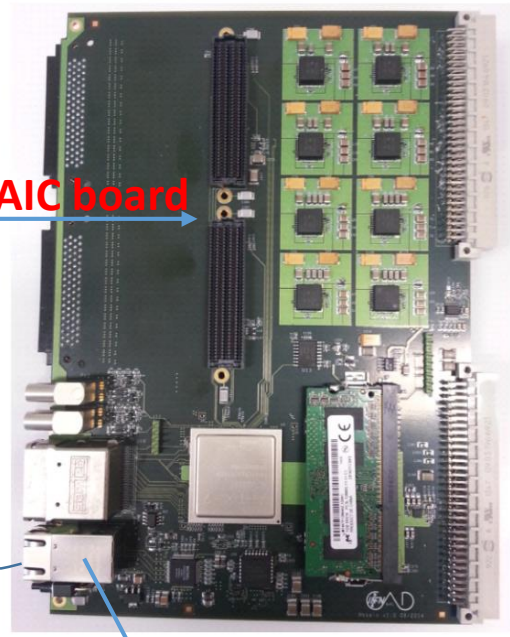


Top view

Test board

FMC connectors

MOSAIC board

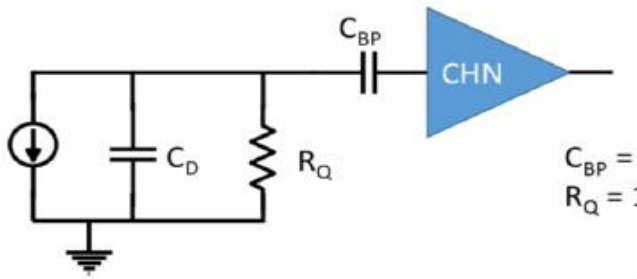


Ethernet port

5 such setup's available at Bari

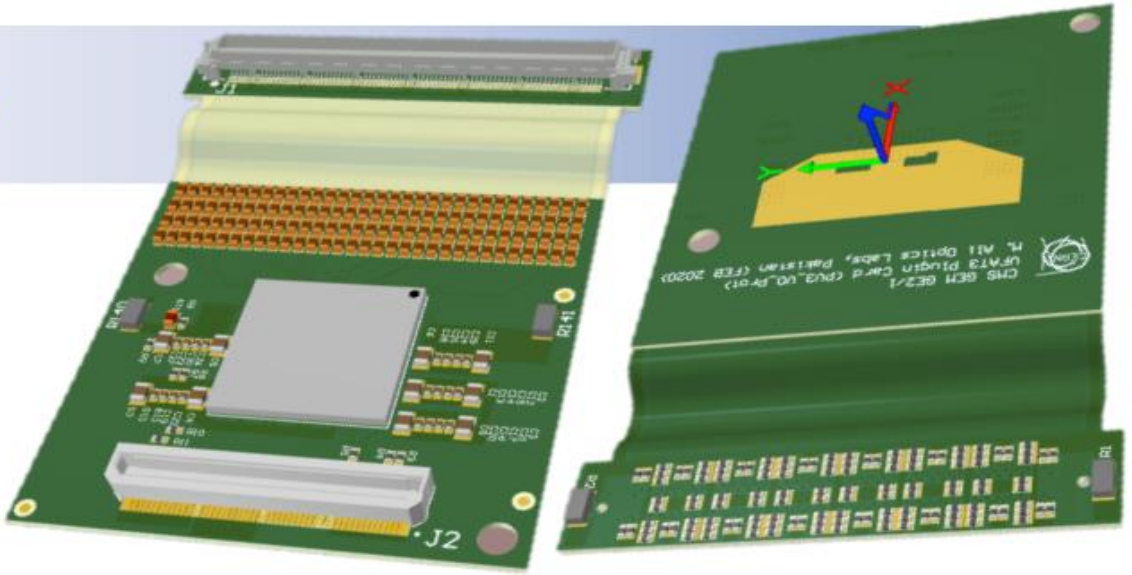
PlugIn Card status

With input protections



C_{BP} = 1 nF
R_Q = 100 kΩ

2



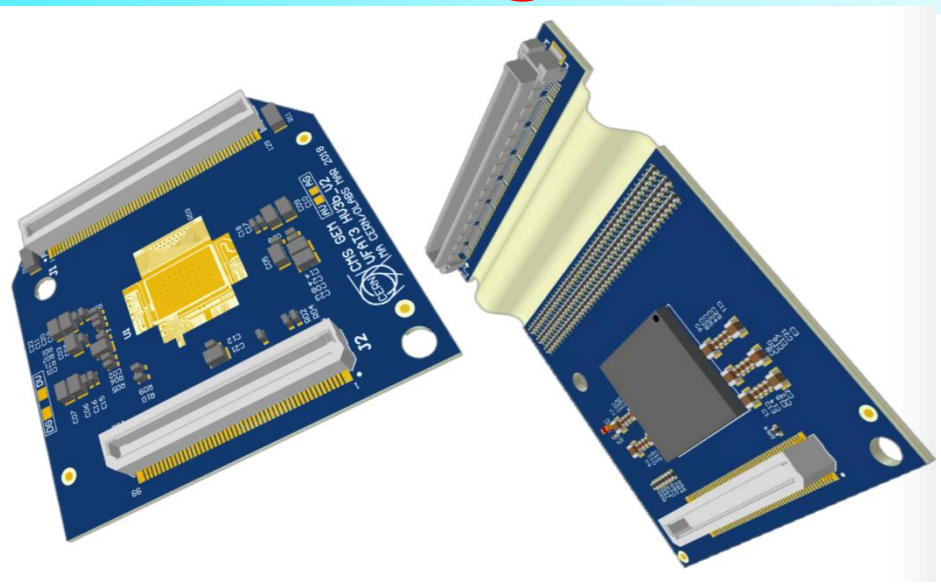
- **A rigid flex single HDI PCB based on packaged VFAT3**
- **The rigid part hosting VFAT3 is plugged on GEB via Panasonic 100-pin connector**
- **The other rigid part has HRS140 connector to ROB**
- **The flex part is capable to accommodate any mechanical misalignment between GEB & ROB**

✓ Version w/o protection: Dec 2019
✓ Version w protection: Feb 2020
✓ Sign-off after review: April 9
✓ Quote query by Jason
✓ Order of 120 cards: May 4

The review twiki

The existing test and verification setup for GE1/1 hybrids may be used for GE2/1 plugin Card

Plug-In card testing



GE1/1 VFAT3 hybrid and GE2/1 Plug-In card are very similar

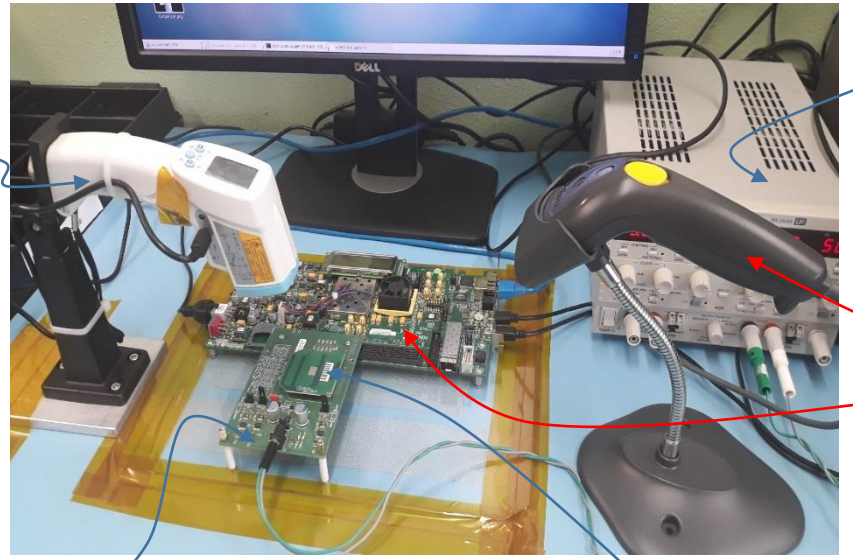
Actually the digital connection to the GEB is the same:

- same panasonic connector
- same pin-out

-> we can re-use the GE1/1 VFAT3 hybrid test bench

More info at:
https://indico.cern.ch/event/912872/contributions/3839170/attachments/2034434/3405715/VFAT3_Production_QC_TestBench.pdf

Hybrid test-bench



Hybrid Labelling

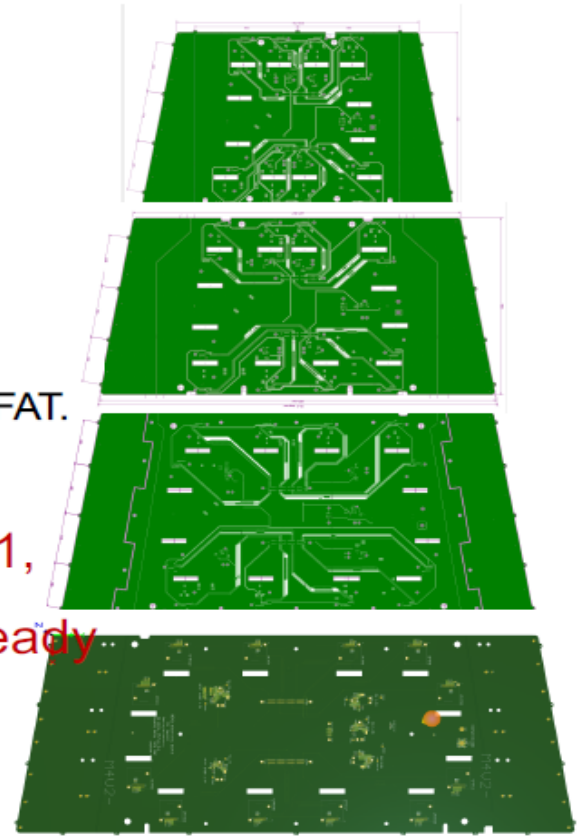
- ~2 minutes Test Time per hybrid
- Online database storage
- 2 set-up's available at CERN

GE2/1 M1-M4 GEB v2: modifications

- with LpGBT compatibility
- VFAT numbering updated; addressing by resistors
- Shielding design was improved a lot considering the mechanic design and chamber operation.
- Improved powering scheme:
  - VDD I/O of 2.5 V powering added in Panasonic connector for each VFAT.
  - 1.2 V Feasts powering VFATs: independently as DVDD and AVDD

✓ Status: M4 design ready on May 8, presented on May 11, waiting for the feedback from reviewers, then it can be ready for production at the end of May

✓ QC & shipment of M1-M4 will be done together.



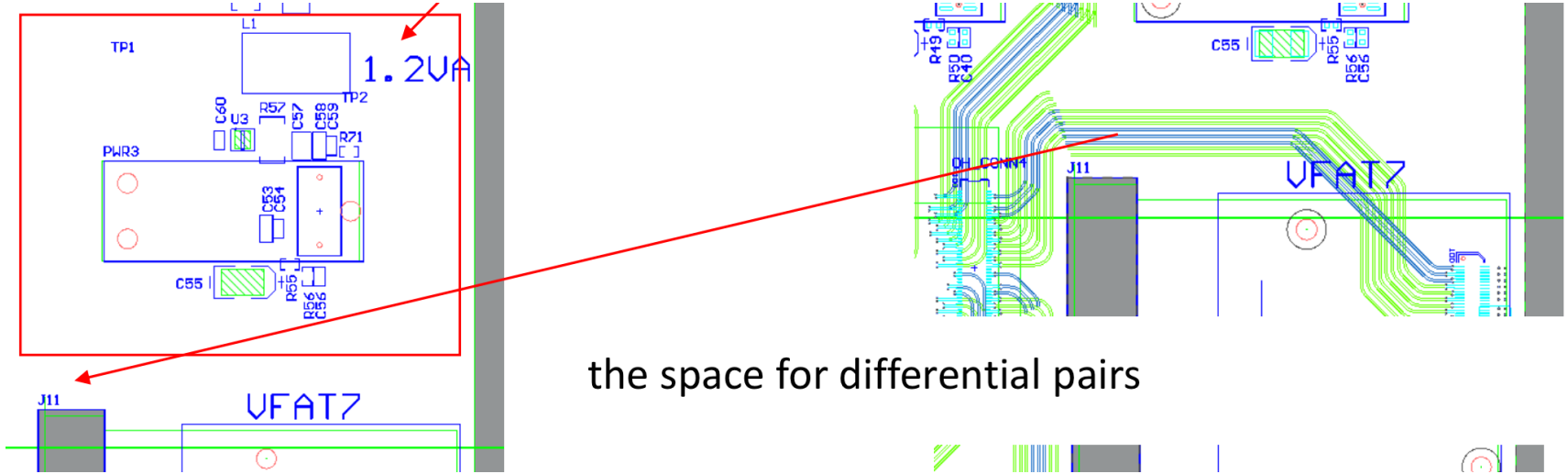
GE2/1 GEB M1-M4 V2 design

Interface Documentation (~30p) is completed and passed several round of review. In final sign-off since April.

ME0 GEB
Electrical Status

- **Two GEB types**
- **Design of smaller (more challenging) GEB**
  - **Routing mostly complete by Zhihua Xue (PKU)**
    - **https://indico.cern.ch/event/917672/ (3rd item)**

- **Big Board! Difficult routing! Example:**

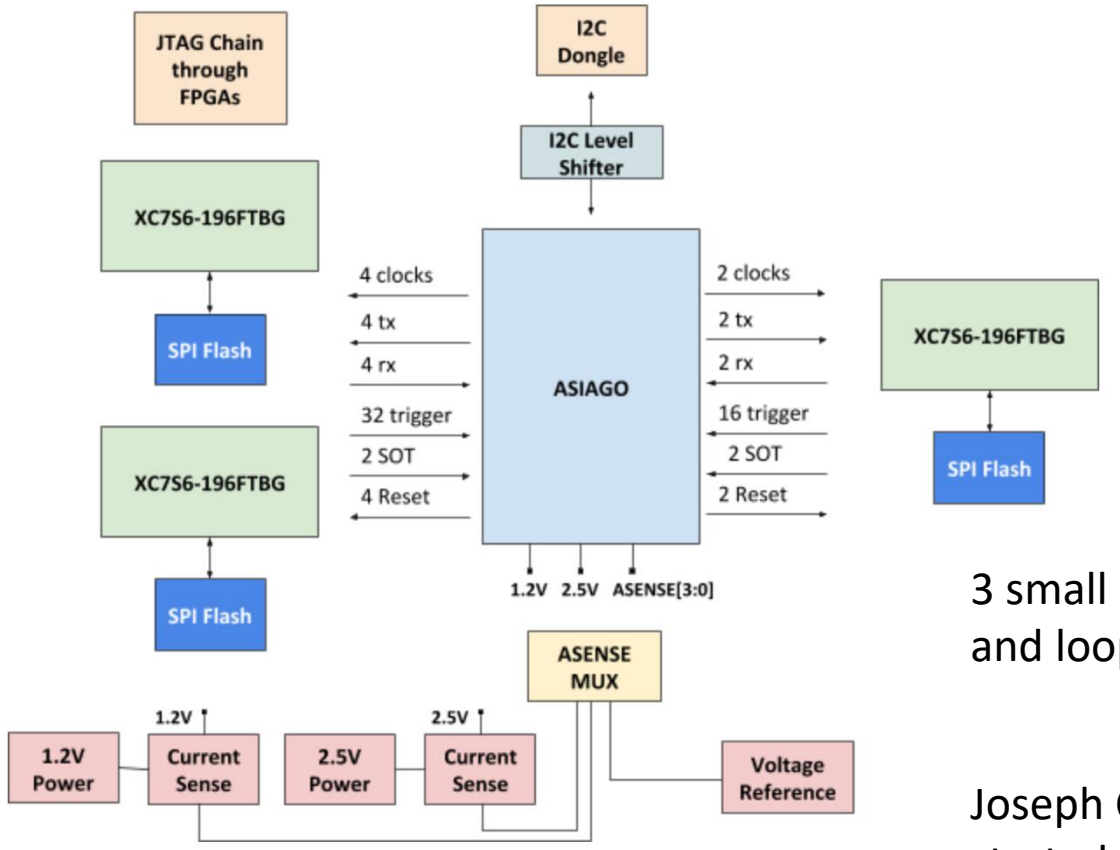


the space for differential pairs

QUESO
(QUalification of Electrical Signals and Optics)

- **An FPGA-based loopback board for efficient standalone production testing of the ASIAGOs"**
  - **Draft spec still as Google Doc (→ Twiki)**

Peck design



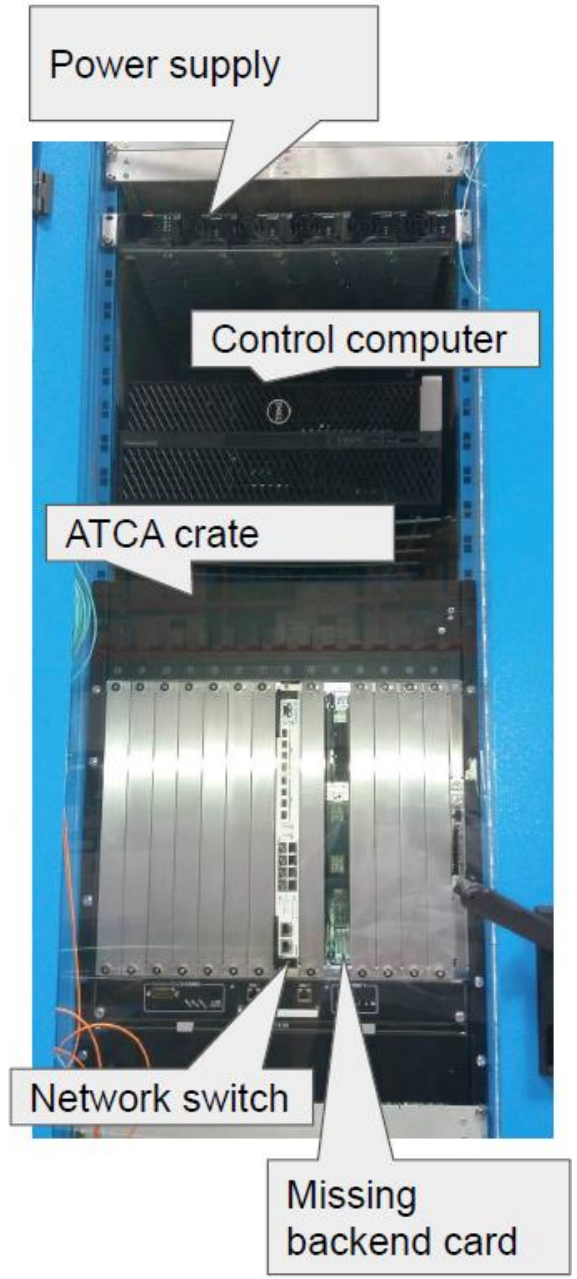
3 small FPGAs receive, fan-out and loop-back to mimic VFATs

Joseph Carlson (UCLA) has started work.

11. ATCA Test Stand at 904

Evaldas Juska (TAMU)

- **Joint GEM/CSC ATCA test stand at 904**
  - Almost all components installed
    - Crate, power supply, network hub, computer
    - Fibers for connecting to GE2/1 superchamber and a full ME0 stack
    - Missing: backend card and DTH
  - Focus on GE2/1 until ESR
  - Then focus on CSC ODMB prototype validation
  - Shared use after that
- **Additional test stands planned**
  - TAMU, UCLA
  - An upgrade to the CERN test-stand, aim to add an extra APT card
  - One more test stand at CERN in 2022
    - GE2/1 test-stand (part of the core cost) and bulk of the ATCA production boards (both GE21 and ME0) arrive in 2022
  - One or more of these can be replaced with multiple PCIe cards that can be distributed to more sites (see later slides)



16. Backend alternative for test stands

Evaldas Juska (TAMU)

- **Bittware CVP13 card selected**
  - Card arrived at TAMU
    - Currently en route to Europe
    - No tests have been done yet
    - Expect news soon
  - Plan to qualify ASAP
    - Order up to 2 more for now
    - One or more of the future ATCA stands could be replaced by these cards
      - One stand buys 6.5 of these
  - Backup available if CVP13 not suitable
    - Alpha Data ADM-PCIE-9H7
    - More links, but higher cost ($9000)
  - Large FPGA -- VU13P
    - 1.5x bigger than the APT ATCA card
  - 16 optical links at 25Gb/s

FPGA	VU13P (-2 speed grade)
FPGA resources	5.5x CTP7 logic cells 1.5x APT (ATCA) logic cells
Optical links	16 (extendable to 32), 25Gb/s 2 ME0 layers 2 GE2/1 chambers
Memory	2x DDR4 DIMMs (300Gb/s)
Copper input	USB-C format Ref clock input + 2 MGTs
Cooling	Water cooling, or passive air
Cost	$5500 (+$300 water cooling) 14% of ATCA stand with APT 23% of uTCA stand with CTP7

18. Summary - Backend

Evaldas Juska (TAMU)

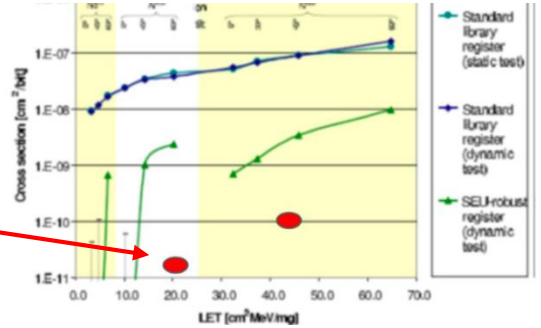
- **Firmware is well advanced**
  - Full support for GE2/1 and ME0 (except sbits) on CTP7
  - Integration with EMTF is progressing well
  - Planned features
    - "Configuration blaster"
      - Automatically configure all GBTs, VFATs, OHs after each hard reset (in 300ms)
    - Support VFAT3 zero suppressed data format
    - Support 3 BX readout
      - VFAT3 doesn't really support it, need to send fake L1As to work around
      - Is it really necessary? We can use pulse stretch feature
      - Study needed (perhaps DPG could help?)
- **Fiber systems are well defined**
- **ATCA developments are ramping up**
  - Test stand at 904 ready
    - Currently waiting for backend card(s)
      - APEX already en route, APT will come soon
    - DTH will come soon as well
  - Looking into PCIe alternatives
    - Bittware CVP13 en route

Irradiation test: SEU

- In November 2019 VFAT3 was irradiated with Heavy Ion Beam to measure SEU x-sections:
  - Slow Control Register
  - SRAM memory

LET [MeV/(mg/cm²)]	Ion	run dose [rad]	mean flux [i/cm² s]	reached fluence [i/cm²]	elapsed time[sec]	Cross section(cm²)
20.4	Ni	979.2	9585	3000051	313	5.4×10^{-11}
46.1	Rh	7382.3	15028	10008557	666	1.6×10^{-10}

Comparison with standard FF



- Good news:
  - SEU x-sections are very small
- Bad news:
  - Observed unexpected losses of synchronization
- Reminder:
  - All logic inside VFAT3 is implemented using TMR.
  - All FF outputs are voted using three independent voters and the three voters outputs are feed back to the three FF. The result is that every clock cycle FFs are updated with the corrected value.

⇒ Planning a new irradiation test at Louvain asap

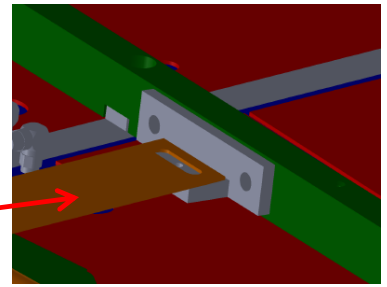
Technical Coordination

Introduction *CERN*	*Michele Bianco*	03:00 - 03:05
Summary of GE2/1 Design and ME0 protyping *CERN*	*Antonio Conde Garcia et al.*	03:05 - 03:30
Design of GE2/1 cooling system *CERN*	*Plamen Iaydjiev et al.*	03:30 - 03:45
ME0 Radmon system *CERN*	*Plamen Iaydjiev et al.*	03:45 - 04:00
GE2/1-ME0 HV Power System *CERN*	*Biagio Rossi et al.*	04:00 - 04:20
GE2/1-ME0 LV Power System *CERN*	*Shimaa AbuZeid*	04:20 - 04:40
GE2/1 RO Fibers procurement and ME0 design *CERN*	*Evaldas Juska*	04:40 - 05:00
Temp Monitor System for Phase 2 GEM projects *CERN*	*Michele Caponero*	05:00 - 05:20
GE2/1 & ME0 gas system *CERN*	*Daniel Francois Teyssier et al.*	05:20 - 05:40
On-Disk Cooling System for GE2/1 & ME0 *CERN*	*Zoltan Szillasi*	05:40 - 06:00
Planning for GE2/1 Demonstrator *CERN*	*Michele Bianco*	06:00 - 06:20

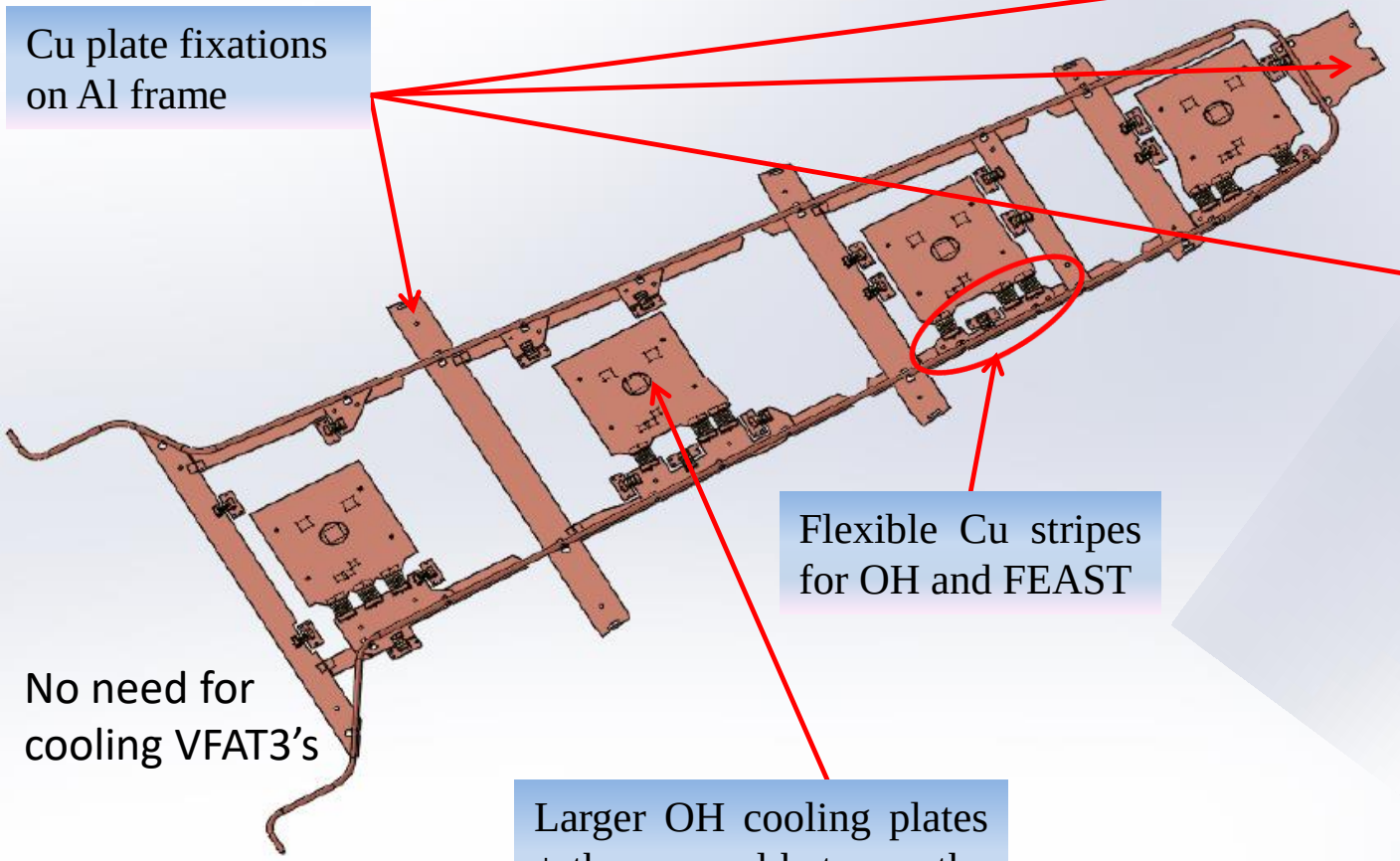
Design of GE2/1 cooling system

Version 2 of the GE2/1 cooling prototype

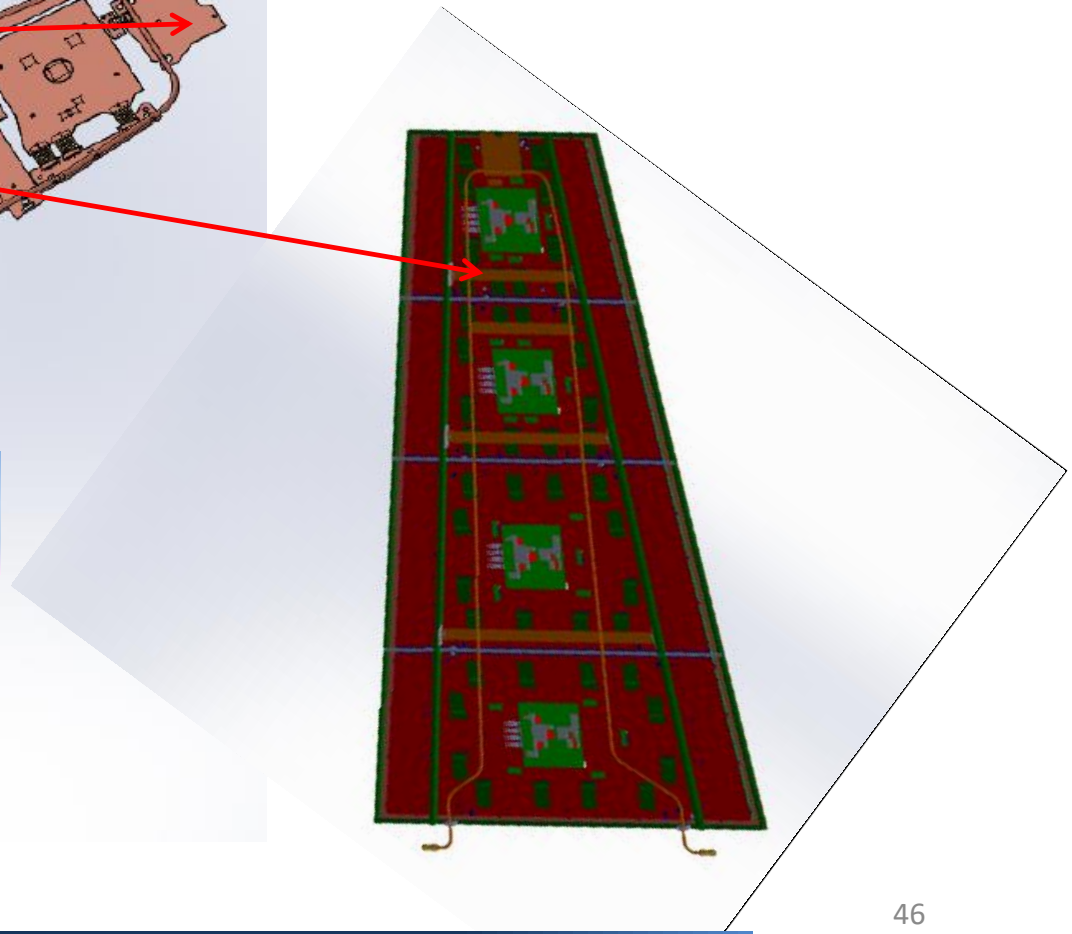
Last check is going on and the second prototype for the test could come to 904 in September 2020 (Covid19 restrictions depending)



Cu plate fixations on Al frame



Flexible Cu stripes for OH and FEAST



No need for cooling VFAT3's

Larger OH cooling plates + thermo pad between the OH and cooling plate

GE2/1 HV

USC

- Rack
- SY4527
- Type 2 Cable
- Patch panel with shield banana connector

UXC

- Racks
- Patch panels
- Type 2 Cable
- Type 3 Cable

Some pictures

USC rack front side

USC rack front side

USC Patch panel front side

UXC X4 rack back side

UXC X4 rack back side

UXC X4 rack front side

Main Phase2 activities affected by COVID-19

Probably not completed list (bias of TC view)

- GE2/1 PCBs (and main components) procurement
- Tests with double segmented foils against discharges and Xtalk in RO
- Discharge tests for hybrid input protection
- ME0 aging tests
- ME0 rate capability studies
- ME0 prototype assembly
- ME0 stack design
- ……

So far no Phase 2 Work Package has been prepared; focus is on GE1/1

Please add/suggest the missing tasks

Summary

- GE1/1 priorities will defined next operations at CERN for GEM group
- Phase2 tasks, in particular detectors R&D, are not running since mid March and will not be possible to resume them before second half of June
- Needs to identify additional space for allow R&D activities to be resumed and keep them running
- Run 3 schedule still unchanged but could be in next months
- Eventual cancellation of 2021 data tacking with 2022 fully dedicated to collisions could require the anticipation of GE2/1 demonstrator

On the side but equally important, preparation of GE2/1 fiber plant lengths to run and succeed with PRR in early July is ongoing final table with validates lengths expected to be ready in one month

GE2/1 Demonstrator in CMS

- If the GE2/1 installation will be anticipated in autumn 2021 seems almost impossible to install a production chambers as GE2/1 demonstrator and even with the current installation schedule (Feb 2022) will be challenging
- One of the two prototype chambers (most likely M5-M8) can be use as GE2/1 demonstrator, in any case equipped with stack realized only with single-segmented foils, probably not the final GEM stack layout
- GE2/1 services, at least on the Neg. End Cap, are almost ready, GE2/1 fibers still to be procured, but readiness should not be an issue for the demonstrator
- Plan for DCS and DAQ deployment not yet discussed, RC workshop in two weeks is a good opportunity to steer the plan

Management & Schedules

Project Schedule	*Alexei Safonov*	
CERN		08:00 - 08:30
Status of Production Sites & New Production Organigram	*Dr Luigi Benussi*	
CERN		08:30 - 08:55
Procurement for Production	*Jeremie Alexandre Merlin*	
CERN		08:55 - 09:20
Database Status	*Adeel Adeel-Ur-Rehman*	
CERN		09:20 - 09:40
Technical Coordination Report	*Michele Bianco*	
CERN		09:40 - 10:10
Upcoming Reviews & Documentation Status	*Prof. Kevin Black*	
CERN		10:10 - 10:30
COVID-19 Impact on Schedules	*All*	
CERN		10:30 - 10:50

GEM Phase-2 Schedule Evolution

- Initial baseline approved in 2017
  - September 2017: CMS Muon Phase-2 Upgrade TDR
- Updates to the “live” schedule as part of the project tracking
  - A number of design developments and improvements, risks realizing including both technical issues as well as vendor delays and funding changes
  - On average, a delay of ~3-6 month for critical delivery dates for the construction project accumulated over the period of 3 years
    - Some intermediate milestones delays as much as 9 month, e.g. GE21 ESR
- A new baseline schedule in 2020:
  - Part of the CMS wide exercise in response to the LHC schedule changes announced at the end of 2019
  - The new baseline captures the status of the project as of early March of 2020
    - A number of changes in planning, installation, need-by dates for installation for both GE21 and ME0
- COVID related delays are tracked relative to the new baseline
  - Effectively we are treating it as a risk that has been realized and we are obviously behind the new baseline:
  - LHC and CMS schedule updates are expected, it is not yet clear if it will amount to a new re-baselining exercise, but it’s likely

GE2/1 R&D Milestones (TDR)

- Up to the start of the construction project

	ID	Milestone title	Date	
Design	GE21.RD.DET.1 GE21.RD.FE.1 GE21.RD.BE.1	GE2/1 R&D: Key detector system design parameters are defined based on performance requirements	21.Mar.17	Achieved
	GE21.RD.FE.2	GE2/1 R&D: On-chamber electronics preliminary design completed and interfaces defined	19.Jun.17	Achieved
	GE21.RD.BE.2	GE2/1 R&D: Off-chamber electronics preliminary design completed and interfaces defined	12.Mar.18	Achieved
	GE21.RD.DET.2	GE2/1 R&D: A full size chamber prototype with partially instrumented readout built, tested and performance validated	1.May.18	Achieved
	GE21.RD.DET.3	GE2/1 R&D: Detector design parameters optimization completed, final chamber design is selected for the demonstrator	8.May.18	Achieved
	GE21.RD.FE.3	GE2/1 R&D: On-chamber electronics prototypes engineering design complete	1.Jun.18	Achieved 28.Sep.18
Prototyping	GE21.RD.FE.4	GE2/1 R&D: On-chamber electronics prototype electronics manufacturing and testing is complete	9.Oct.18	Achieved 19.Feb.19
	GE21.RD.DET.4	GE2/1 R&D: Performance of the demonstrator chamber with prototype electronics is validated	12.Mar.19	Achieved 17.May.19
	GE21.RD.FE.5 GE21.RD.BE.3	GE2/1 R&D: On-chamber and off-chamber prototype electronics integration and performance studies completed	12.Dec.19	New baseline: Aug.20
		GE2/1 PRR for the On-Detector Services	3.Aug.2018	Achieved (Jul.18)
		GE2/1 PRR for the Foil Production	13.Nov.2018	Achieved 22.May 19
		GE2/1 Detector EDR	12.Mar.2019	Achieved 22.May.19
		GE2/1 ESR	12.Dec.2019	New Baseline: Aug.20

GE21 Construction (TDR)

- Update of the GE21 milestones table from the TDR
  - Later milestones have been set by the expected at the time of the TDR lack of availability of the backend electronics
  - We should review that part of the schedule further

		GE2/1 PRR for the On-Detector Services	3.Aug.2018	
		GE2/1 PRR for the Foil Production	13.Nov.2018	
		GE2/1 Detector EDR	12.Mar.2019	
		GE2/1 ESR	12.Dec.2019	
Production	GE21.PR.DET.1	GE2/1 On-Disk Services Installation Complete	20.May.2019	NB: 3.Jul.2020
	GE21.PR.FE.1	GE2/1 On-Chamber Electronics Manufacturing and Testing is Completed	3.Mar.2021	NB: 20.Jul.2021
	GE21.PR.DET.2	GE2/1 Chambers for Disk-1 are assembled, tested, and ready for installation	16.Nov.2021	NB: 25.Jan.2022
	GE21.PR.DET.3	GE2/1 Module manufacturing and testing is complete	8.Feb.2022	NB: 09.Aug.2022
	GE21.PR.DET.4	GE2/1 Chambers for Disk-2 are assembled, tested, and ready for installation	5.Apr.2022	NB: 04.Oct.2022
	GE21.PR.BE.1	GE2/1 Off-Chamber Electronics Manufacturing & Testing completed and ready for installation	5.May.2023	NB: 06.Jul.2023
		GE2/1 Full Detector Commissioning Starts	15.Mar.2024	NB: 03.Jul.2024

ME0 R&D Milestones (TDR)

- Up to the start of the construction project

	ID	Milestone title	Date	
Design	ME0.RD.DET.1 ME0.RD.FE.1 ME0.RD.BE.1	ME0 R&D: Key detector system design parameters are defined based on performance requirements	21.Mar.17	Achieved
	ME0.RD.DET.2	ME0 R&D: Irradiation studies and assessment of performance and longevity with small prototypes completed	11.Jul.2017	Achieved
	ME0.RD.FE.2 ME0.RD.BE.2	ME0 R&D: On-chamber & off-chamber electronics preliminary principal design complete and interfaces defined	25.Jul.17	Achieved
	ME0.RD.DET.3	ME0 R&D: Chamber (stack) prototype mechanical design completed	18.Dec.2018	Achieved
	ME0.RD.FE.3	ME0 R&D: On-chamber electronics engineering design completed and validated	23.Aug.2019	NB: 21.Aug.2020
Prototyping	ME0.RD.DET.4	ME0 R&D: Chamber (stack) prototype mechanical prototype testing and validation complete	24.Dec.2019	NB: 13.Apr.2020
	ME0.RD.FE.4	ME0 R&D: On-chamber electronics prototype electronics manufacturing and testing is complete	21.Aug.2020	NB: 8.Jan.2021
	ME0.RD.BE.3	ME0 R&D: Integration of the on-chamber and off-chamber electronics and performance assessment complete	8.Jan.2021	NB: 02.Apr.2021
	ME0.RD.DET.5 ME0.RD.FE.5	ME0 R&D: Assessment of the electronics performance and integration with the demonstrator chamber completed	30.Mar.2021	NB: 28.May.2021
	ME0.RD.DET.6	ME0 R&D: Beams and Cosmics testing of the demonstrator chamber and performance qualification completed	31.Aug.2021	NB: 29.Oct.2021
		ME0 PRR for the Foil Production	14.Jun.2021	NB: unchanged
		ME0 ESR	27.Apr.2021	NB: 01.Dec.2021
		ME0 Detector EDR	28.Oct.2021	NB: unchanged

GE21 Construction Schedule

- Key dates:
  - Foil production completed: Apr.29.2022
  - Production of the modules start - end: Jan.29.2021- Aug.09.2022
  - Chamber assembly: Sep.03.2021 – Oct.04.2022
  - Need-by date for ready for installation: Oct.02.2023
- Critical path (given assumptions):
  - Module assembly driven by the components availability
    - India's funding a key concern: prior to COVID, the plan was to exercise fallback options to fund Drift/RO boards PCBs, if no clear resolution by the end of April 2020
- Other concerns:
  - Electronics for chamber assembly has only two months of float, very likely to get on critical path
    - Potential to speed this up via a PRR for OHs
      - Starting GEB production in Fall is realistic, but requires some inventive steps as full funding will likely not yet be available, but PKU colleagues are optimistic that this will happen
        - Firm news on PKU funding in the summer

ME0 Construction Schedule

- Key dates:
  - Foil production completed: Apr.14.2023
  - Production of the modules start - end: Nov.02.2022- Jul.23.2024
  - Chamber assembly: Jan.25.2023 – Oct.05.2024
  - Need-by date for ready for installation: Dec.31.2025
- Critical path (given assumptions):
  - Module assembly driven by the components availability
  - Chamber (stack assembly) becomes part of the critical path towards the very end of the project
- Other concerns:
  - Electronics for chamber assembly has four months of float, likely to get on critical path
  - GE21 delays can have a very direct impact on ME0 schedule, especially module assembly

Thank you!

The End

Backup

GEM Foil Production at CERN

Producer: MPT workshop (a.k.a Rui's lab) based at CERN

Item	Quantity needed	Quantity ordered	Quantity received	Quantity tested
M1	108	111	19	0
M4	108	111	0	0
M5	108	111	54	18
M8	108	111	0	0

Production report: production rate is about 40 foils per month. 1-3 foils per batch have to be returned for advanced cleaning → consistent with GE11 experience

Validation report: test rate is not optimal at the moment and will become worst when Korean foils will arrive at CERN → increasing test stand capacity and implement parallel testing

Current Status: on hold, waiting for the validation of the new design (see X-talk issue presentations)

GEM Foil Production at Mecaro

Producer: Mecaro, based in Korea

Item	Quantity needed	Quantity ordered	Quantity received	Quantity tested
M2	108	111	0	0
M3	108	111	0	**0**
M6	108	111	0	0
M7	108	111	0	0

Internal review: organized in Korea in January 2020
https://twiki.cern.ch/twiki/bin/view/CMS/ReviewMecaro

Current Status: mass production on hold, waiting for the validation of the new design (see X-talk issue presentations)

Pending issues: production of M7 foils for aging studies. This R&D production should also demonstrate that Mecaro was able to fix the problems spotted during the review

Foils design / Rate Capability

Medium-term R&D program

- ***New ME0 prototype with the foils in final configuration***
  - Tests for: rate capacity, discharge/propagation probability, etc.
  - New rate capability measurement
    - Final protection resistors value
    - Optimization high-voltage resistive filter

Medium-term R&D program

- ***Test Beam for rate capability (muon detection efficiency)***
- 1st option: test at ***CERN CMS GEM QA/QC facility*** (904 Lab.)
  - cosmic-ray muon with an Ag-target X-ray generator as background source
- 2nd option: muon test beam at ***CERN GIF++ facility***
  - muon beam from the SPS, ^{137}Cs as background source
- **Both option require: tracking chamber** (two 10 cm×10 cm triple-GEM detectors), and **two scintillators** as a trigger for the muon tracking (plus control / RO electronics)

3 Plans for Aging test @ Korea

- Aging test of Korean foils will be performed at UoS
  - Same procedure
  - All equipment are available except for the x-ray gun and chamber

- Purchasing process of x-ray gun ongoing
  - Got Permission from KINS (Dec. 19)
  - Halted due to fiscal year changing. Resumed
  - Logistic problem due to COVID19. At least 2 months or more
  - Not enough to cover 7.9 C/cm^2

ASIAGO

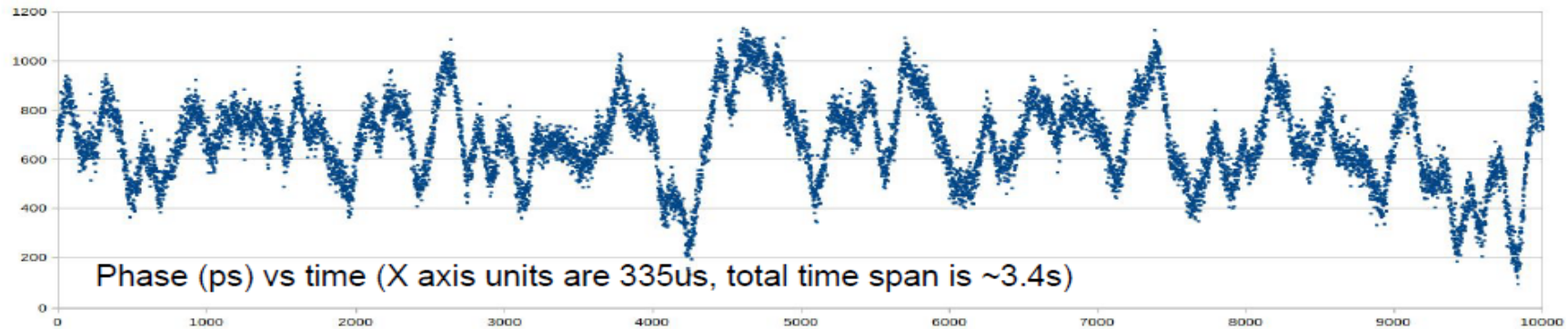
- ASIAGO= ME0 OptoHybrid
- _v1 finished at UCLA (Peck) some time ago.
  - Link between VFAT3 & LpGBT verified
  - Used a Firefly & later VL+ optics to readout
- _v2 a small change to be done by B.U.
  - (still Peck)
- Joseph Carlson (new engineer @ UCLA) working on schematics for tester board (QUESO)
  - Saltzberg/Carlson meeting regularly with Peck
- Many tests:
  - https://twiki.cern.ch/twiki/bin/viewauth/CMS/ME0ASIAGO#Testing

9. Recent CTP7 firmware updates

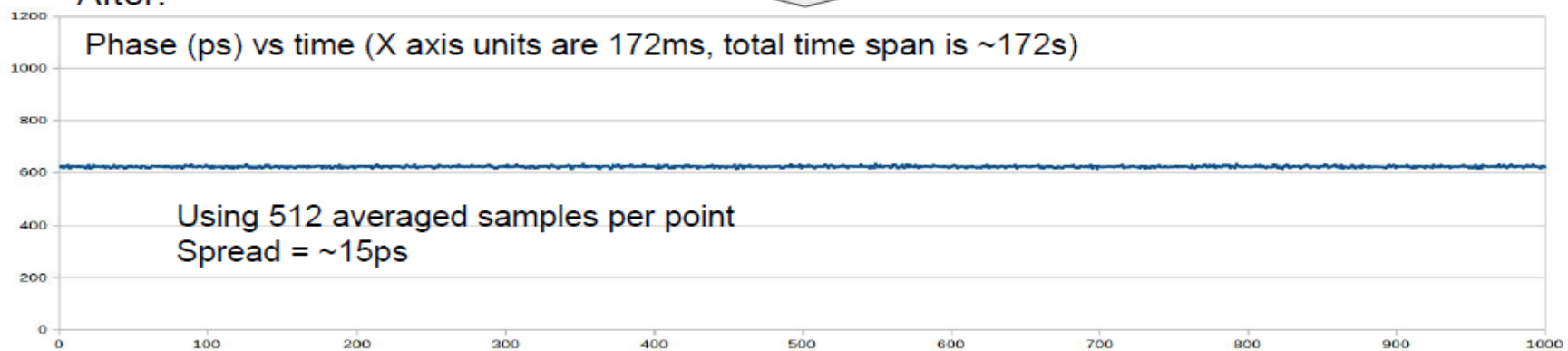
Evaldas Juska (TAMU)

- **Clock phase monitoring and alignment to CMS phase**
  - Phase monitoring has been significantly improved
    - Using DMTD method, same as on TCDS system (more info in this paper)
    - Include configurable averaging
      - Allows trading off measurement time vs accuracy
    - Measurement spread can be as low as 15ps
  - Precise phase locking with configurable offset

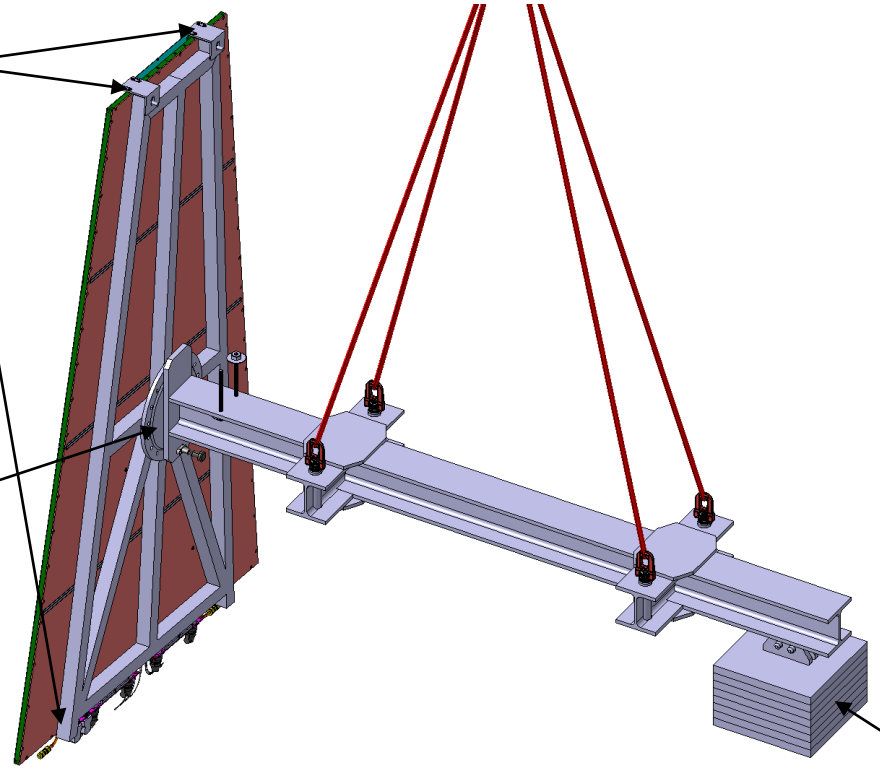
Before:



After:



Hoisting beam



4 attachment points

Pivot placed in the center of gravity of the chamber in order to easily select the good angle

Fixed counterweight

-DESIGN SIMILAR TO EXISTING GE1/1 LIFTING BEAM

-VERY STABLE: 4 SUSPENSION POINTS

Summary

- Summary of GEM GE2/1 & ME0 gas system readiness:
- Gas system hardware is already installed for GE2/1 for both endcaps
- All 18×2 lines gas leak tested and distribution racks commissioned with bypasses. The final commissioning will require the volume of the detectors.
- The infrastructure of the system, ie. mixer, pumps and pre-distribution racks is already in use in GE-1/1 and running. GE2/1 and ME0 will use the same infrastructure.