



Testing of GE2/1 & ME0 GEM detectors for CMS Phase-2 Muon System Upgrade

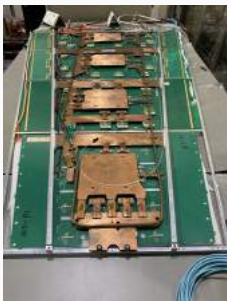
Bandar Alsufyani, Stephen Butalla, Marcus Hohlmann, & **Erick Yanes**
on behalf of the CMS Muon Group

April, 26th 2023

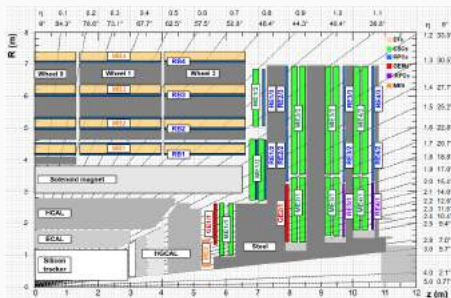
Florida Institute of Technology
APS April Meeting April 2023



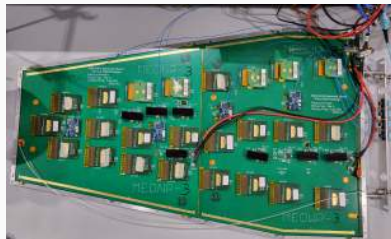
- The LHC's High Luminosity (HL) upgrade will increase its instantaneous luminosity by five-fold
- So CMS is improving its muon spectrometer with the addition of new Triple-GEM detectors (GE2/1 and ME0)
- GE2/1 and ME0 are in the production and prototype stages respectively



GE2/1

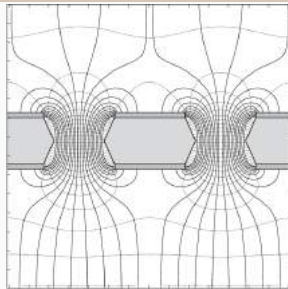


Cross-section of CMS quadrant [1]



ME0

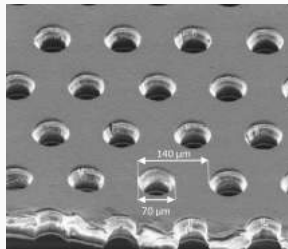
- The Gas Electron Multiplier (GEM) is made out of a metal-clad polymer foil with an extremely dense array of holes
- High-energy charged particles entering the chamber leave behind energy deposits in the form of free electrons and ions.
- Electrons and ions are accelerated by an electric field inside the holes
- A primary electron can knock other electrons, forming a cascade known as a *Townsend Avalanche*
- Of Course, we'll need a way to read such signals.



Electric Field of a GEM foil [2]



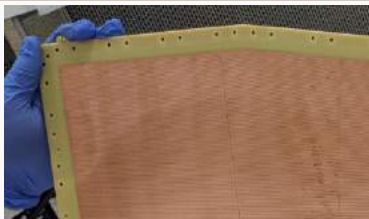
A GEM Foil for ME0



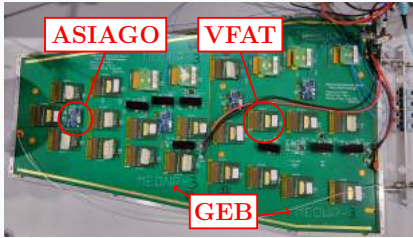
Hole Size on GEM Foils [3]

Read Out Board (ROB) and GEM Electronics Board (GEB)

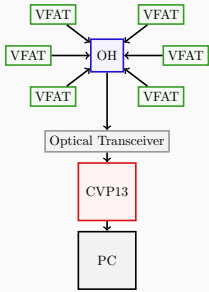
- Analog signal (charge) is induced on one of the strips on the ROB and then measured by the VFAT3 frontend chip
- The GEB will route the digital signal from the VFAT3 to the ASIAGO Optohybrid (OH)
- ASIAGOs transmit data through optical fibers to Optical transceivers
- Optical transceivers plug into CVP13 FPGA-based backend processor card, which handles a majority of our processing
- How are the front chip electronics tested?



Strips on ROB



ME0



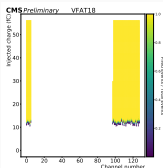
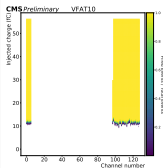
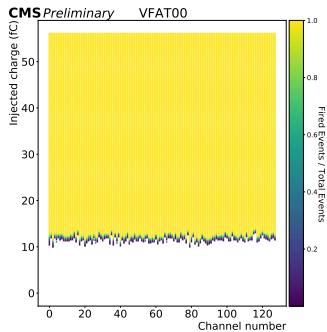
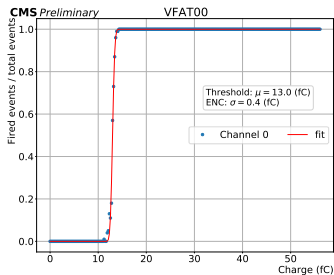
Communications from ROB to the PC



Optical transceivers plugged into the CVP13

S-Curves and Missing Channels

- VFATs are tested by injecting charge into each of 128 channels, and fitting them into an S-Curve
- A voltage comparator should only respond when the injected charge exceeds a certain threshold
- Issue was seen at FIT, and later CERN, that channels will randomly go missing
- Missing channels always appeared in pairs, and mostly occurred on ASIAGO 2
- Found mismatch errors also appeared in pairs



| VFAT num | Mis-match |
|----------|-----------|
| 2 | -2 |
| 3 | -2 |
| 10 | 20751 |
| 11 | -14032 |
| 18 | 20751 |
| 19 | -14032 |

Solving the problem of the missing channels

- Forward Error Corrections (FECs) were also seen on ASIAGO 2
- The high light output of old optical transceivers modules is the cause of the FECs hence missing channels
- So the solution is to reduce the light output power coming from the optical transceiver
 1. Using an attenuator to reduce the light power on ASIAGO 2, see the table below.
 2. Using a low light output
- **No missing channels were found over 40 consecutive S-Curves for ASIAGO 2 or any other ASIAGO.**
- Backends at FIT and CERN now use special lower-power optical transceivers

| Downlink | |
|----------|------|
| ASIAGO | FECs |
| 1 | 519 |
| 2 | 1563 |
| 3 | 0 |
| 4 | 0 |

| ASIAGO 2 Downlink | | | |
|-------------------------|--------------|------|---------|
| Power (μW) | Duration (h) | FECs | FECs/h |
| 850 | 1 | 39 | 39 |
| 800 | 1 | 17 | 17 |
| 700 | 24 | 106 | 4.4167 |
| 650 | 24 | 27 | 1.125 |
| 600 | 13 | 4 | 0.308 |
| 550 | 12 | 0 | < 0.083 |



Old Higher-Powered optical transceiver



New Lower-Powered optical transceiver

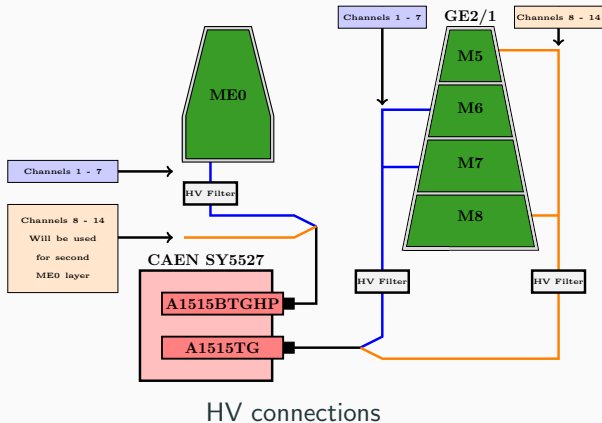
Quality Control on M8 – Hardware & Software for High Voltage

Hardware:

- Mainframe CAEN SY5527 houses both the low voltage board and two high voltage boards
- Each CAEN HV board has 14 channels, split into two groups of seven
- Seven channels control one layer of ME0 or two modules of GE2/1

Software:

- LabVIEW programs perform four quality control tests: Stress Test, IV-Scan, Short Stability Test, and Long Stability Test
- Software records the parameters over time of the channels
- A local Grafana instance plots the current & voltage of the channels over time

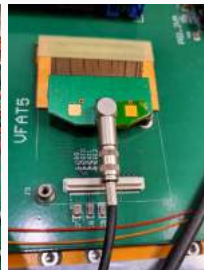


Quality Control on M8 – Monitoring System

- **REPORT** When applying HV, the front chips got dead channels or resetting due to discharges.
- So, we start to investigate the discharges in the chamber:
 - a) Four HV probes are connected to four of the foils (to monitor the voltage of the foils)
 - b) Magnetic probe to measures the currents in the **ground line** of the ROB
 - c) Five ganged output strips measure the voltage on the ROB



Magnetic Probe



Ganged Output Cable



HV Oscilloscope and
Magnetic Probe Oscilloscope



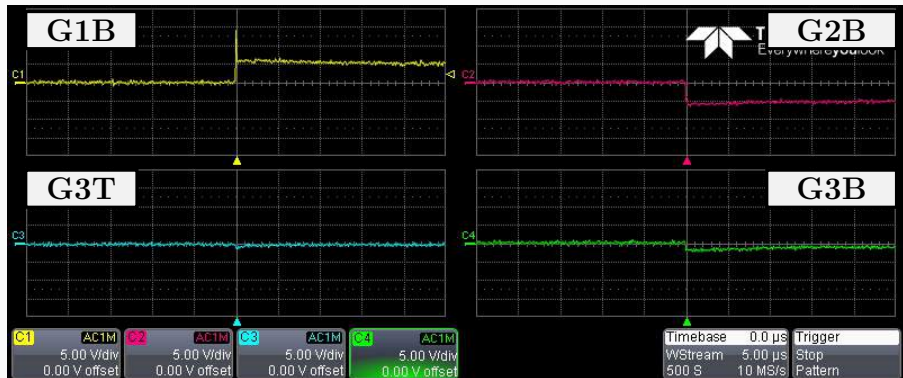
4 Readout Sectors Monitored on Scope

Quality Control on M8 – Stress Test – Discharges

- The stress test's purpose is to determine the highest voltage that can be applied to each GEM foil without damaging them (without discharges)
- No discharge upto 550 V
- However, start seeing some discharge at 600 V on a single foil
- Discharges can be seen in Grafana

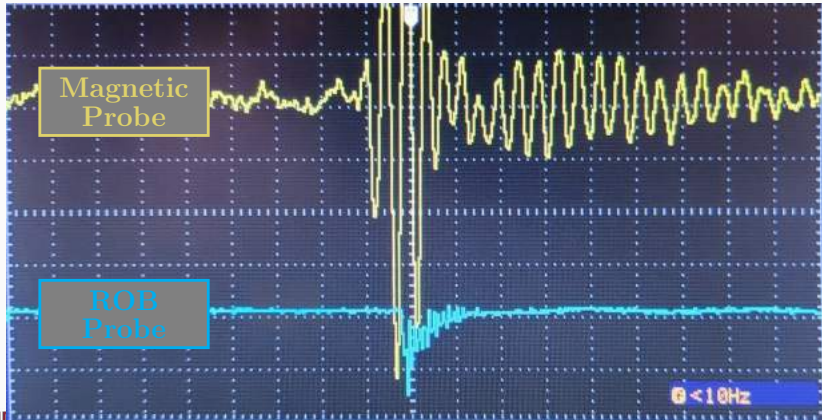


Voltage on the GEM Foils during a Discharge



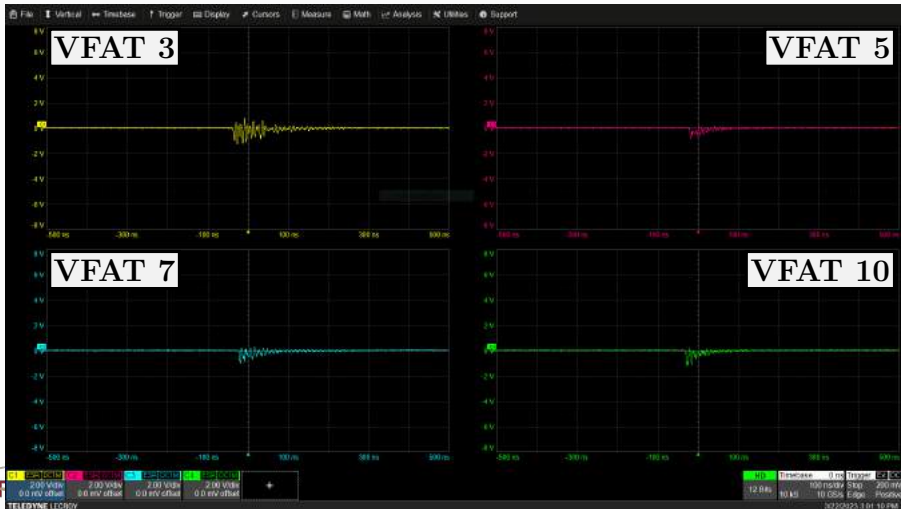
Discharge on G2T propagates to the other foils

- Detect a current flow through the grounding line when discharge occurs:
 - ◇ 20mA per division, -100mA at the peak
 - ◇ This current could possibly flow to the frontend electronics and potentially cause dead or reset the channels
- Also detected voltage on ROB probe due to that discharge:
 - ◇ Unfortunately, the scale is unknown for the ROB probe



Magnetic Probe and one ROB Probe during Discharge

- Output voltage when discharge occurs on the ROB:
 - ◇ As we see one discharge effect many ROB sectors
 - ◇ Still do not know under which VFAT the discharge happens



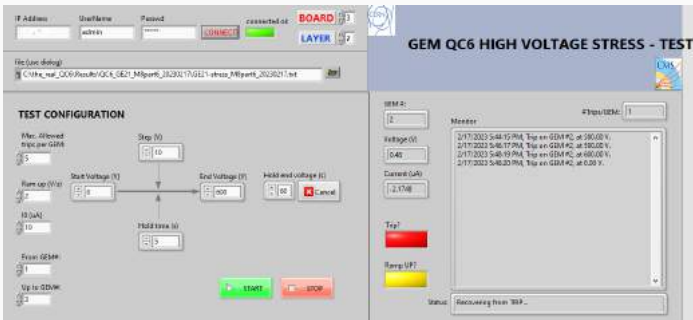
- The FECs and resulting missing channels are due to the high light output of optical transceivers:
 - ◇ Using low-power Vitex optical transceivers, we were able to fix the problem of missing channels
- The M8 module passed the Stress test, although discharges are occurring at 600 V
- Investigating the cause of lost channels and resetting the front chips during HV by:
 1. Monitoring the voltages of the foils
 2. Monitoring the currents through ground lines
 3. Monitoring the voltage seen by the ganged sectors
- Results of the discharge investigation:
 - ◇ Discharges on one foil affect the other foils
 - ◇ Discharges also create ground currents and a voltage on the ROB, both of which can possibly affect our frontend electronics

- [1] CMS Collaboration, *The Phase-2 Upgrade of the CMS Muon Detectors: Technical Design Report*, [CERN-LHCC-2017-012](#), [CMS-TDR-016](#), (2017).
- [2] Buzulutskov, Alexey. (2007). Radiation detectors based on gas electron multipliers (Review). *Instruments and Experimental Techniques*. 50. 287-310. 10.1134/S0020441207030013.
- [3] CMS GEM Collaboration, CMS technical design report for the muon endcap GEM Upgrade , [CERN-LHCC-2015-012](#), [CMS-TDR-013](#), Jun 2015,

Backup

Quality Control on M8 – Stress Test – overview

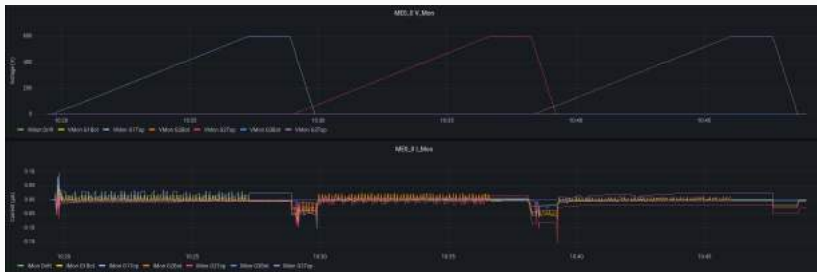
- **Purpose:** The stress test's purpose is to determine the highest voltage that can be applied to each GEM foil without damaging them
- **Procedure:**
 1. Scan the voltage range from 0 to 600V in 10 V steps for top GEMs, then hold the step for one minute, then back to zero.
 2. Writing down the number of trips
 3. A successful test is when first the max voltage is greater than 500V, and the recorded trips are less than 5 trips.



Stress Test Detect Discharges (trips)

CMS student work in progress

Quality Control on M8 – Stress Test – Grafana instance



CMS student work in progress

Quality Control on M8 – Monitoring System

