Calculation and Measurement of the Interstrip Capacitance and Its Correlation With Measured ENC for the CMS GE2/1 GEM Detector

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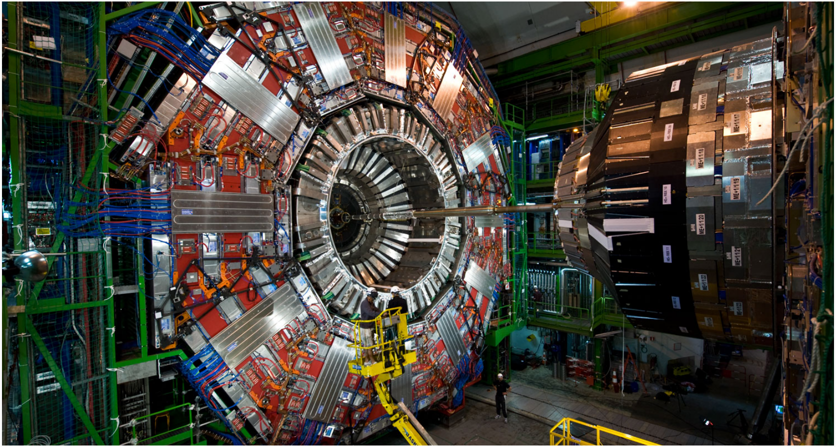
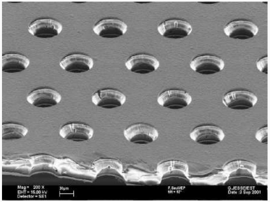
The Muon System of the CMS Experiment



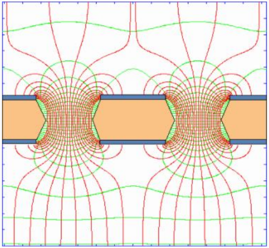
The Compact Muon Solenoid [1].

Gas Electron Multipliers

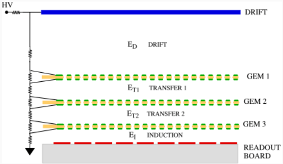
- CMS gas electron multipliers (GEMs) are micro-pattern gas detectors (MPGD) that consist of three foils inside an active volume filled with gas (a mix of 70:30 Ar/CO_2)
- The foils are held at different potentials through a high voltage (HV) divider



Electron microscope image of a GEM foil [2].



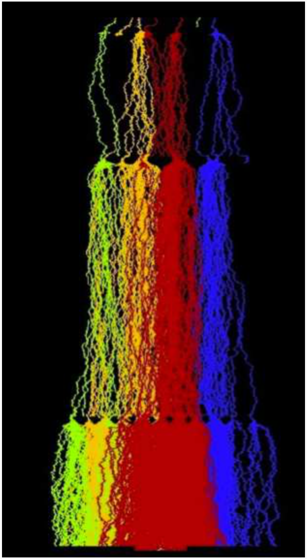
Electric field and potential from the GEM foil [2].



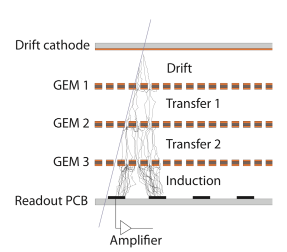
Schematic of the foils in the detector [2].

Gas Electron Multipliers

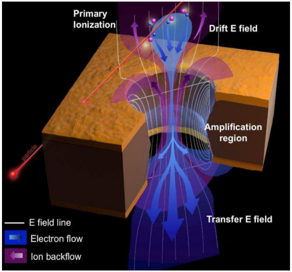
- As a particle (or photon) enters the detector, it ionizes the gas
- Free electrons accelerated by electric fields cause secondary ionization inside the holes in the foils ($|\mathbf{E}|$ can be as high as 10^7 V/m!) $\Rightarrow$ creates an avalanche
- Charge is collected on the strips on the readout board (ROB) which is then integrated by the readout electronics



Simulation showing charge multiplication between GEM foils [3].



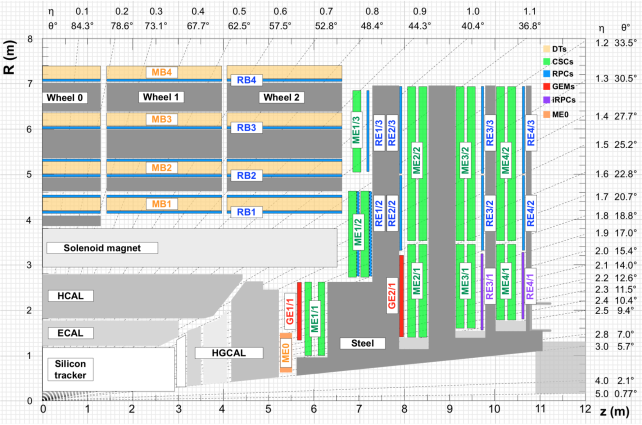
Electron avalanche
and gain multiplication between GEM foils [3].



Ionization process and charge amplification [3].

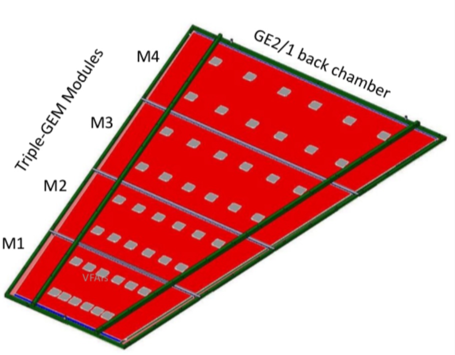
Phase-II Upgrade for CMS

- High Luminosity LHC project (HL-LHC) will increase luminosity $\sim \times 5$
- The Phase-II muon detector upgrade will help increase the redundancy of the muon system
- GE2/1 will help control the Level-1 trigger rate



Muon system for the proposed Phase-II upgrade [4].

The GE2/1 Detector

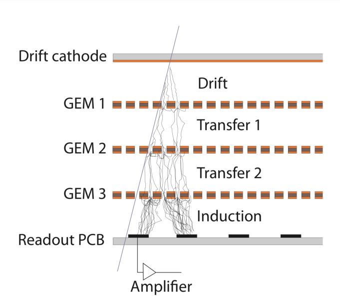


Schematic of the GE2/1 detector [4].

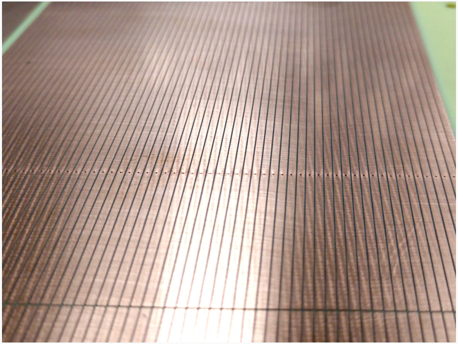
First fully assembled GE2/1 chamber [5].

Interstrip Capacitance of the GE2/1 Readout Board

- Interstrip capacitance is an important design parameter
- Lower interstrip capacitance = lower noise ⇒ higher S/N
- Interstrip capacitance influenced by strip length, width, gap width, dielectric substrate, and signal trace dimensions/geometry
- A custom GE2/1 readout board (in the shape of a GE1/1 readout board) was fabricated with twelve different strip geometries and dimensions
- Physical measurements of the interstrip capacitance were made on this board
- Analytical calculations performed



Schematic of drift, GEM foils, and readout board in the chamber.

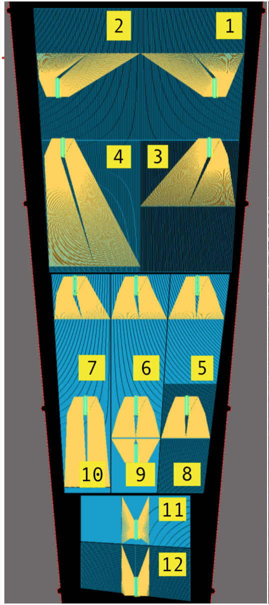


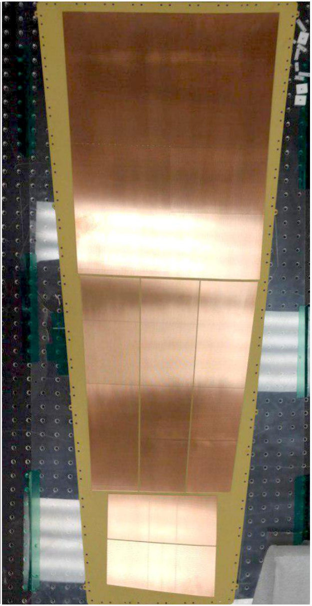
Close-up of readout strips.

Layout of the GE2/1 Readout Board

1. M4, Original TDR Design (Strip gap: 0.2 mm)
2. M4, Strip gap: 0.3 mm
3. M4, Strip length halved, neighbors merged (width doubled), (new default)
4. M4, Extra long traces
5. M1, Original TDR Design (Strip gap: 0.2 mm)
6. M1, Strip gap: 0.3 mm
7. M1, Strip gap: 0.4 mm
8. M1, Strip length halved, neighbors merged (width doubled)
9. M1, Strip length halved, original width
10. M1, Extra long traces
11. M1, Minimal traces
12. M1, Minimal traces, strip length halved, width doubled

Figure on left adapted from [6].





Calculation of the Interstrip Capacitance

- Expression for interstrip capacitance/cm obtained from [7] and modified to include the signal traces on the opposite side of the board

$$(C/l) = \left(C_{\mathrm{strip/sub}} + C_{\mathrm{strip/air}}\right) l_s^{-1} + \left(C_{\mathrm{trace/sub}} + C_{\mathrm{trace/air}}\right) l_t^{-1}$$

- Capacitance terms are functions of the complete elliptic integral of the first kind and dielectric constant
- Moduli of the integrals are functions of the strip and trace dimensions/geometry and substrate thickness
- Trace widths, gap widths, and lengths were measured 24 times in each sector; an average and its standard deviation were calculated

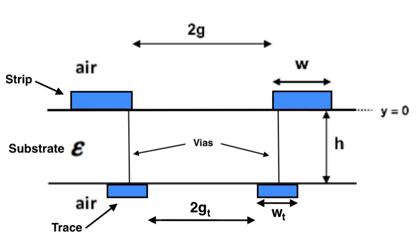
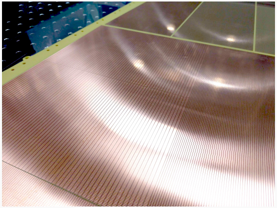
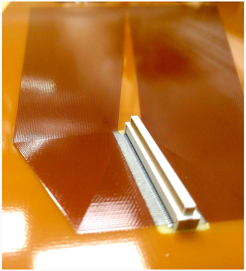


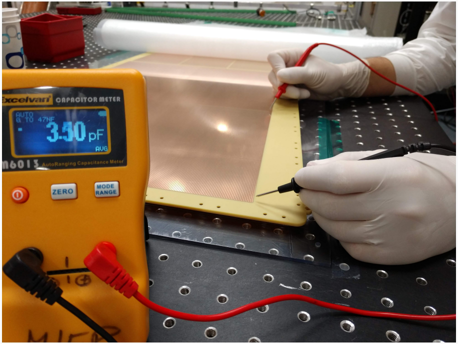
Diagram of the strip/trace/substrate system.


Readout strips.


Signal traces and Panasonic connector.

Measurement of the Interstrip Capacitance

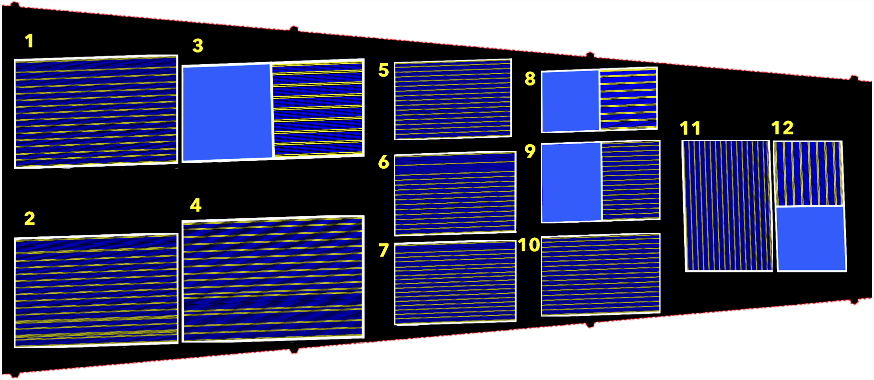
- Probes of the capacitance meter (Excelvan m6013) were placed at opposite ends of two adjacent strips
- The meter was zeroed by a second person while the probes were held ∼1 cm above the strips, then a measurement was taken



- Four measurements taken for 8-22 pairs of strips in each of the 12 sectors on the readout board
- We calculated the weighted mean and its standard error over all trials

Measurement of the Interstrip Capacitance

- In the following discussion, the weighted average of capacitance of all strips measured in each sector is used as the capacitance figure of merit
- Maps of what strips were measured for each sector are shown below [8]; (Yellow lines indicate strip pairs that were measured)



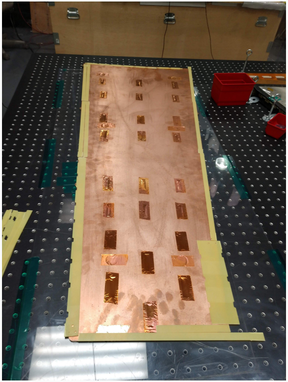
Interstrip Capacitance of the GE2/1 Readout Board

Table 1: GE2/1 ROB Interstrip Capacitance (Work in Progress)

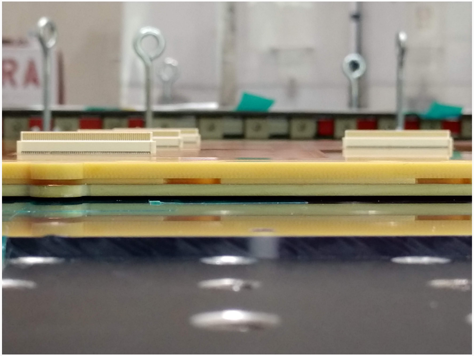
Sector	Module	Parameters	Avg. Meas. Cap. (pF)	Calc. Cap. (pF)	(C_m/C_c)
1	M4	Original TDR Design (Strip gap: 0.2 mm)	21.69±0.05	16.7	1.30
2	M4	Gap: 0.3 mm	19.98±0.12	15.3	1.31
3	M4	2xWidth, 0.5xLength	15.33±0.03	10.5	1.46
4	M4	Original TDR Design, Long traces	27.87±0.06	21.1	1.32
5	M1	Original TDR Design (Strip gap: 0.2 mm)	16.27±0.04	12.7	1.28
6	M1	Gap: 0.3 mm	14.65±0.07	11.2	1.31
7	M1	Gap: 0.4 mm	13.17±0.04	10.6	1.24
8	M1	2xWidth, 0.5xLength	11.82±0.06	8.5	1.39
9	M1	0.5xLength	9.32±0.05	5.9	1.58
10	M1	Original TDR Design, Long traces	20.58±0.06	15.3	1.35
11	M1	Original TDR Design, Minimal traces	14.02±0.02	11.8	1.19
12	M1	Minimal traces, 0.5xLength, 2xWidth	10.39±0.07	7.6	1.37

Measuring the Interstrip Capacitance with GEM3 Bottom Simulated

- To simulate the capacitance contribution from GEM3 bottom, a PCB with solid copper surface was held 1 mm below the readout board with FR4 spacers
- The previous measurement procedure was repeated for each strip pair in all sectors, but with probe contact made from the signal trace side
- We calculated the weighted mean and its standard error over all trials



Copper-covered PCB with FR4 spacers.



Readout board held 1mm above the copper-covered PCB.

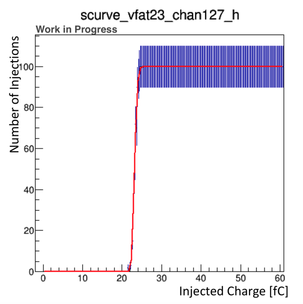
Interstrip Capacitance of the GE2/1 Readout Board

Table 2: GE2/1 ROB Interstrip Capacitance With and Without Copper Plate (Work in Progress)

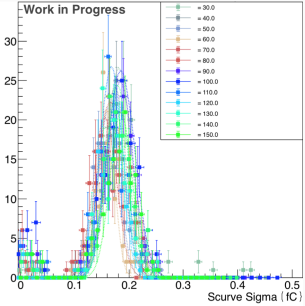
Sector	Module	Parameters	Avg. Meas. Cap. w/o plate (pF)	Avg. Meas. Cap. w/plate (pF)	$(C_w/C_{w/o})$
1	M4	Original TDR design (Strip Gap: 0.2 mm)	21.69±0.05	25.85±0.27	1.192±0.013
2	M4	Gap: 0.3 mm	19.98±0.12	20.98±0.03	1.050±0.006
3	M4	2xWidth, 0.5xLength	15.33±0.03	20.16±0.04	1.315±0.004
4	M4	Original TDR Design, Long traces	27.87±0.06	28.43±0.07	1.020±0.003
5	M1	Original TDR design (Strip Gap: 0.2 mm)	16.27±0.04	19.04±0.21	1.170±0.013
6	M1	Gap: 0.3 mm	14.65±0.07	18.26±0.06	1.246±0.007
7	M1	Gap: 0.4 mm	13.17±0.04	14.85±0.08	1.128±0.007
8	M1	2xWidth, 0.5xLength	11.82±0.06	15.82±0.32	1.338±0.028
9	M1	0.5xLength	9.32±0.05	9.17±0.10	0.984±0.012
10	M1	Original TDR design, Long traces	20.58±0.06	26.80±0.14	1.302±0.008
11	M1	Original TDR design, Minimal traces	14.02±0.02	14.82±0.03	1.057±0.003
12	M1	Minimal traces, 0.5xLength, 2xWidth	10.39±0.07	10.33±0.11	0.994±0.013

Equivalent Noise Charge Measurements

- Equivalent noise charge (ENC) is the noise present in the detector preamplifier/amplifier combination
- S-curves taken at CERN [9]
- S-curve (ENC) measurement consists of injecting a calibration pulse into one channel and recording whether the voltage comparator responds at a given threshold [10]
- Measurements repeated for all channels and fit to a modified error function [10]
- S-curve sigmas were plotted and fit with a Gaussian [9]



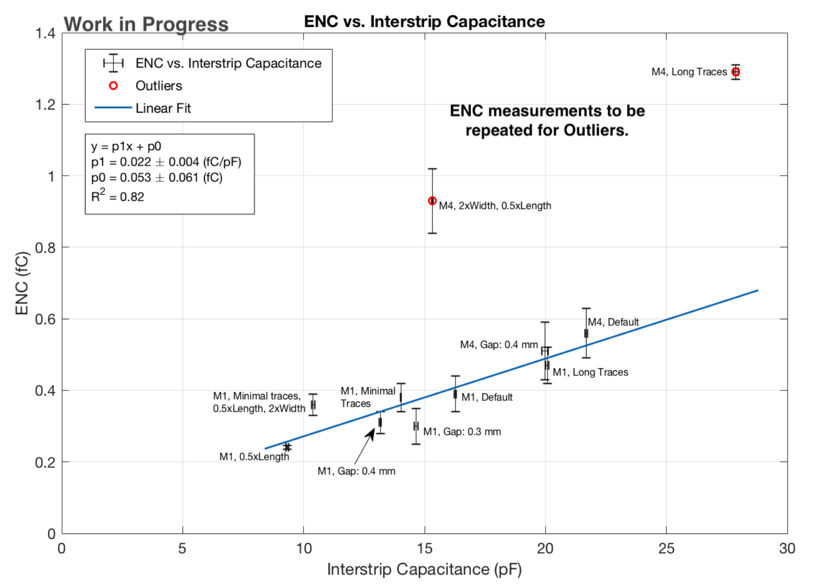
Typical S-curve measurement [10].



Typical S-curve sigma distribution for different voltage comparator levels [9].

Interstrip Capacitance and ENC Comparison

- All ENC measurements obtained from [9]

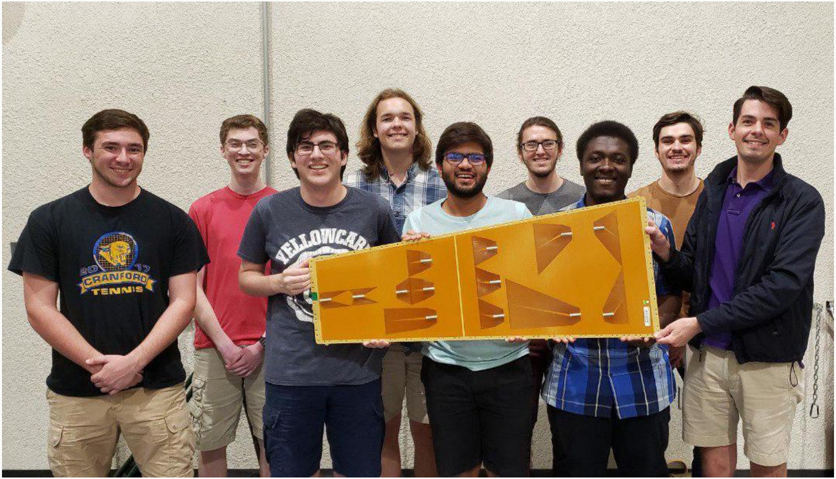


Conclusions

- $\sim$30% discrepancy between calculation and measurement $\Rightarrow$ likely due to the simple model; 128 strips/traces per sector, but only two strips/traces are accounted for in the calculation
- The predicted "best" strip geometries produce the lowest capacitance measured:
  - Measured interstrip capacitance of M4 module with 2xWidth, 0.5xLength reduced by $\sim$30% compared to original design
  - Measured interstrip capacitance of M1 module with 0.5xLength reduced by $\sim$40% compared to original design (also lowest ENC)
  - These designs adopted by CMS
- Traces introduce a non-negligible capacitance to the overall interstrip capacitance $\Rightarrow$ trace length should be minimized
- Capacitance contribution from simulated GEM3 bottom increases interstrip capacitance by $\sim$ 15% on average
- Measured ENC is well correlated with interstrip capacitance; for every pF increase, the ENC rises by 0.022 fC ($\sim$ 131 e^-)

Acknowledgements

- We would like to acknowledge Jerry Collins, Angelo Lucciola, Michael Werbiskis, Dev Roy, Joey Weatherwax, Alex Busto, John Hammond, and Liam Shaw for their help with the measurements of the interstrip capacitance.



References

[1] Image obtained from http://www.hephy.at/en/research/cms-experiment-at-lhc/.

[2] "CMS Detector Design," http://cms.web.cern.ch/news/cms-detector-design.

[3] CMS Collaboration, "CMS Technical Design Report for the Muon Endcap GEM Upgrade," Technical Report CERN-LHCC-2015-012, CMS-TDR-013, CERN, 2015.

[4] CMS Collaboration, "The Phase-2 Upgrade of the CMS Muon Detectors Technical Design Report," Technical Report CERN-LHCC-2017-012, CMS-TDR-016, CERN, 2017.

[5] Photo courtesy of M. Bianco.

[6] A. Ovcharova, "GEM Readout Board Design: Overview and Status," Presentation at the GEM Workshop XXII, https://indico.cern.ch/event/722089/contributions/3041863/attachments/1672580/2684057/18-06-21_ana_RO_boards_status.pdf.

[7] S. Gevorgian and H. Berg, "Line Capacitance and Impedance of Coplanar-strip Waveguides on Substrates with Multiple Dielectric Layers," *31st European Microwave Conference, IEEE (2001)*, doi:10.1109/EUMA.2001.339161.

[8] Figure courtesy of J. Collins.

[9] B. Stone "Noise on GE2/1 Strips ROB," Internal CMS Presentation at the GEM Phase-2 Electronics Meeting: Triad, https://indico.cern.ch/event/771676/contributions/3206497/attachments/1749508/2834310/VFAT_Noise_GE21StripsROB.pdf.

[10] B. Dorney, "Explanation of S curve Fit Algorithim," Internal CMS Presentation at the GEM Phase-2 Electronics Meeting, https://indico.cern.ch/event/780422/contributions/3252280/attachments/1771243/2879820/BDorney_GEMDAQMtg_20181213_SCurve.pdf.

[11] L. M. Milne-Thomson, L. M. (1969). Ch. 17 from *Handbook of Mathematical Functions With Formulas, Graphs, and Mathematical Tables, 9th ed*. Eds. Abramowitz, M. and Stegun, I. A. p. 590. National Bureau of Standards: Washington, D.C.

Appendix B: Full Analytical Expression for Interstrip Capacitance

Adapted from [7]:

$$(C/l) = \left(C_{sa} + C_a\right) l_s^{-1} + \left(C_{st} + C_t\right) l_t^{-1}$$

$$= \epsilon_0 \left((\epsilon - 1) \frac{K(k')}{2K(k)} + \frac{K(k'_{0s})}{K(k_{0s})} \right) + \epsilon_0 \left((\epsilon - 1) \frac{K(k'_t)}{2K(k_t)} + \frac{K(k'_{0t})}{K(k_{0t})} \right)$$

$$k = \tanh\left(\frac{\pi g}{2h}\right) \coth\left(\frac{\pi(w+g)}{2h}\right), \qquad k' = \sqrt{1-k^2}$$

$$k_{0s} = \frac{g}{w+g}, \qquad k'_{0s} = \sqrt{1-k_0^2}$$

$$k_t = \tanh\left(\frac{\pi g_t}{2h}\right) \coth\left(\frac{\pi(w_t+g_t)}{2h}\right), \quad k'_t = \sqrt{1-k_t^2}$$

$$k_{0t} = \frac{g_t}{w_t+g_t}, \qquad k'_{0t} = \sqrt{1-k_{0t}^2}$$

where $K(k)$ is the complete elliptic integral of the first kind, w is the strip width, $2g$ is the gap width between the strips, w_t is the trace width, $2g_t$ is the gap width between the traces, h is the thickness of the substrate (FR4 with dielectric constant $\epsilon = 4.7$).

Appendix C: Complete Elliptic Integral of the First Kind

- The complete elliptic integral of the first kind is given in [11] as

$$K(k) = \int_0^1 \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}}$$