Frontend Electronics Integration for the GE2/1 GEM Detector for the Phase-2 Muon System Upgrade of the CMS Experiment

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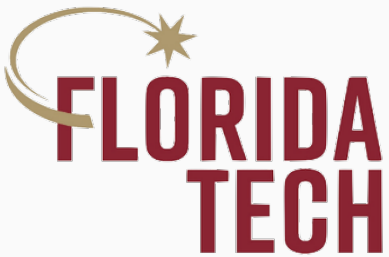
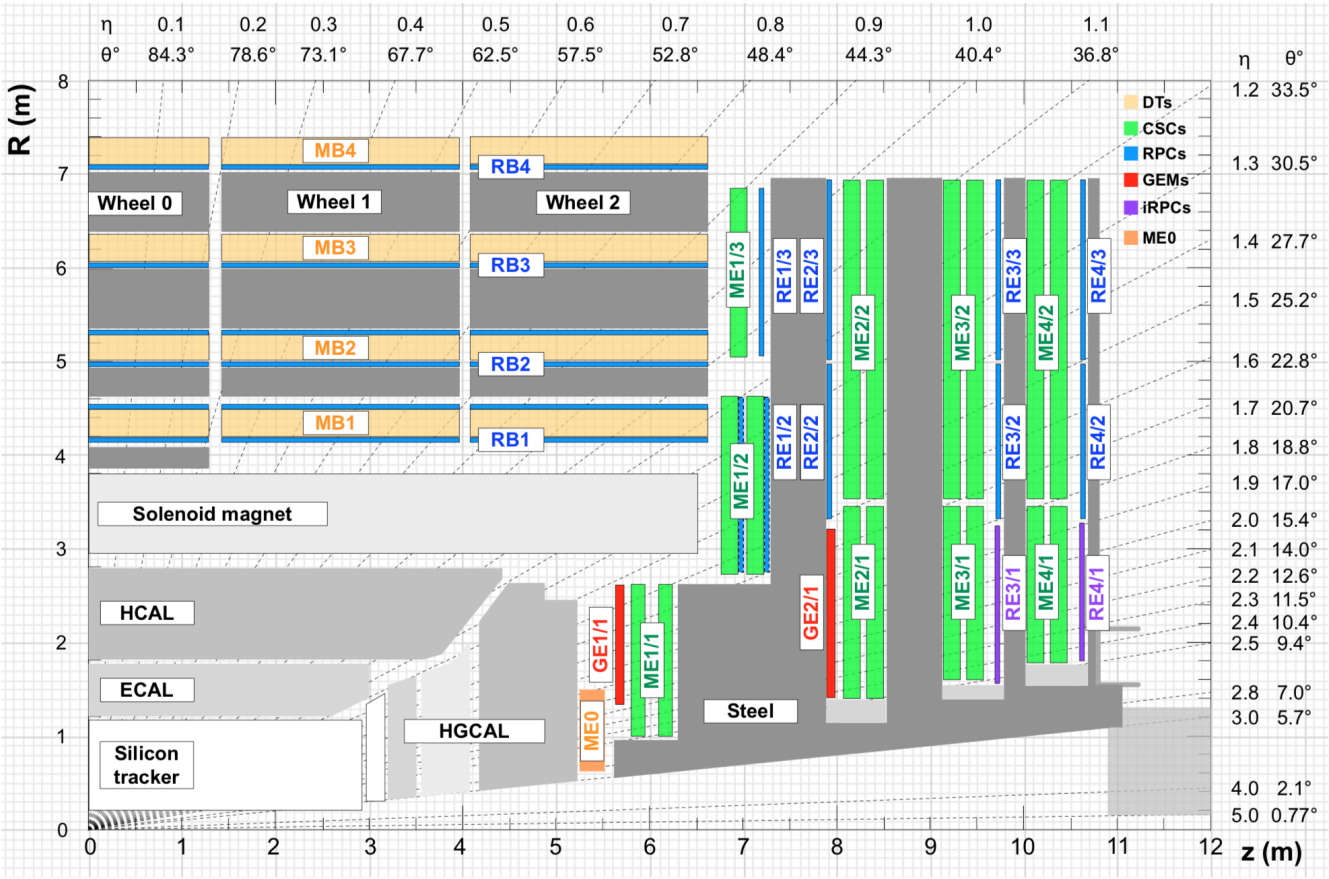


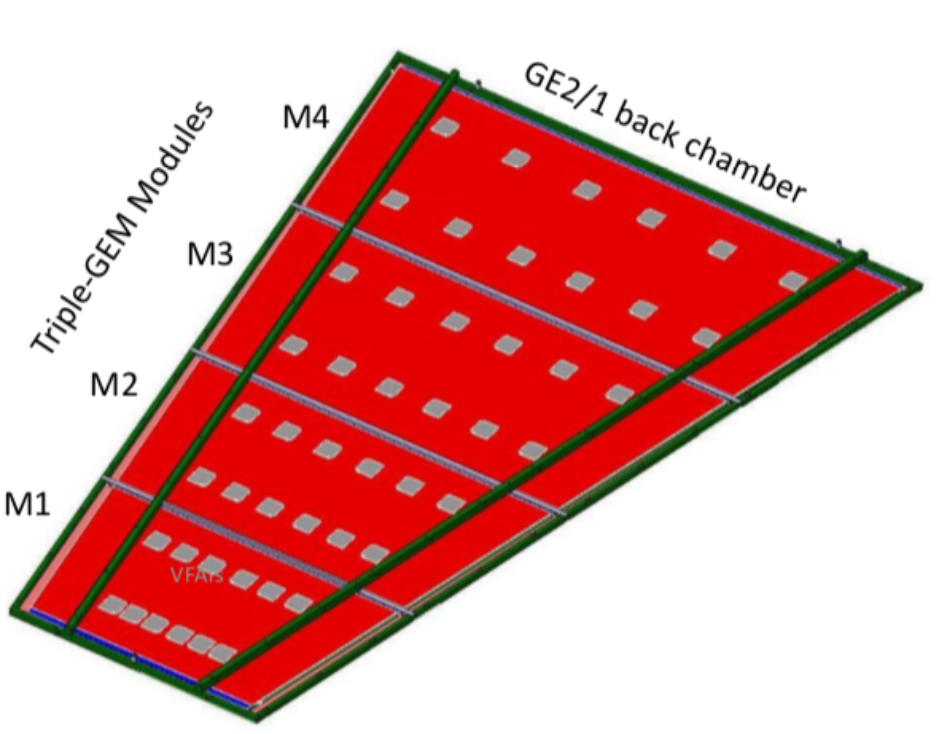
Phase-II Upgrade for CMS

- High Luminosity LHC project (HL-LHC) will increase luminosity $\sim \times 5$
- The Phase-II muon detector upgrade will help increase the redundancy of the muon system
- GE2/1 will help control the Level-1 muon trigger rate

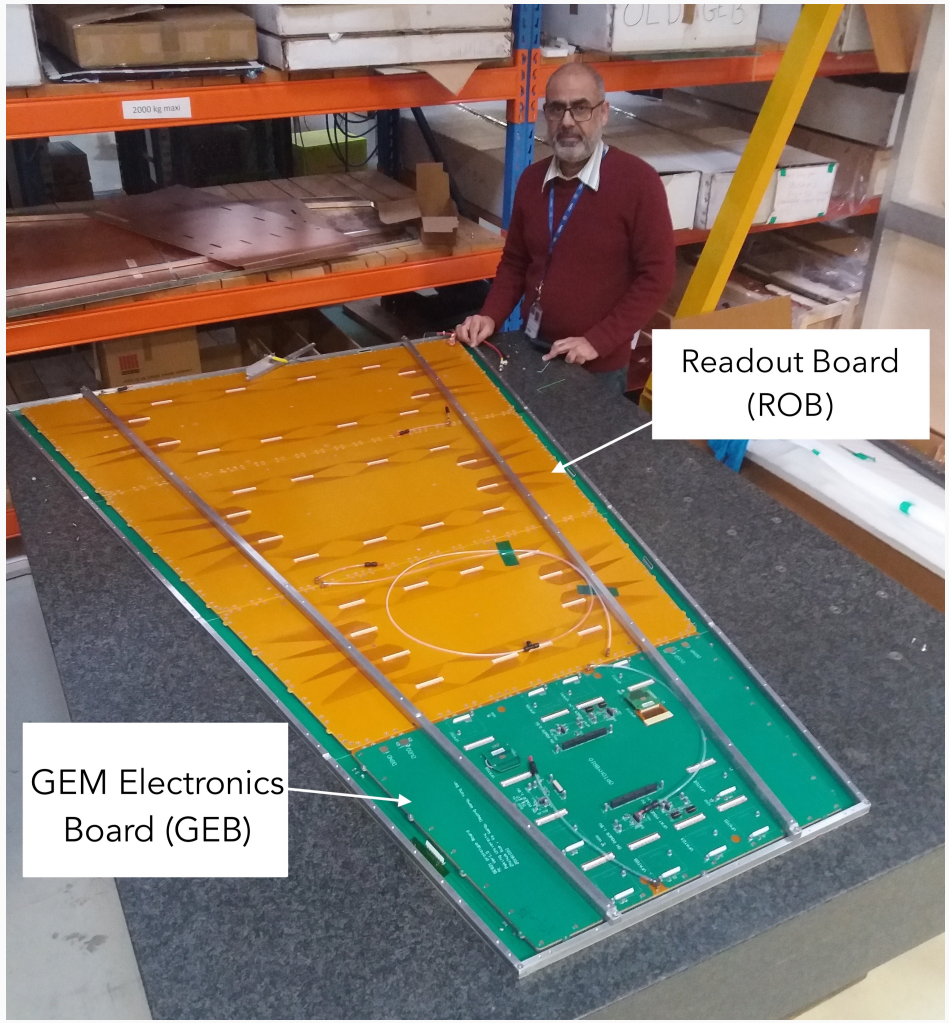


Muon system for the proposed Phase-II upgrade [1].

The GE2/1 Gas Electron Multiplier Detector



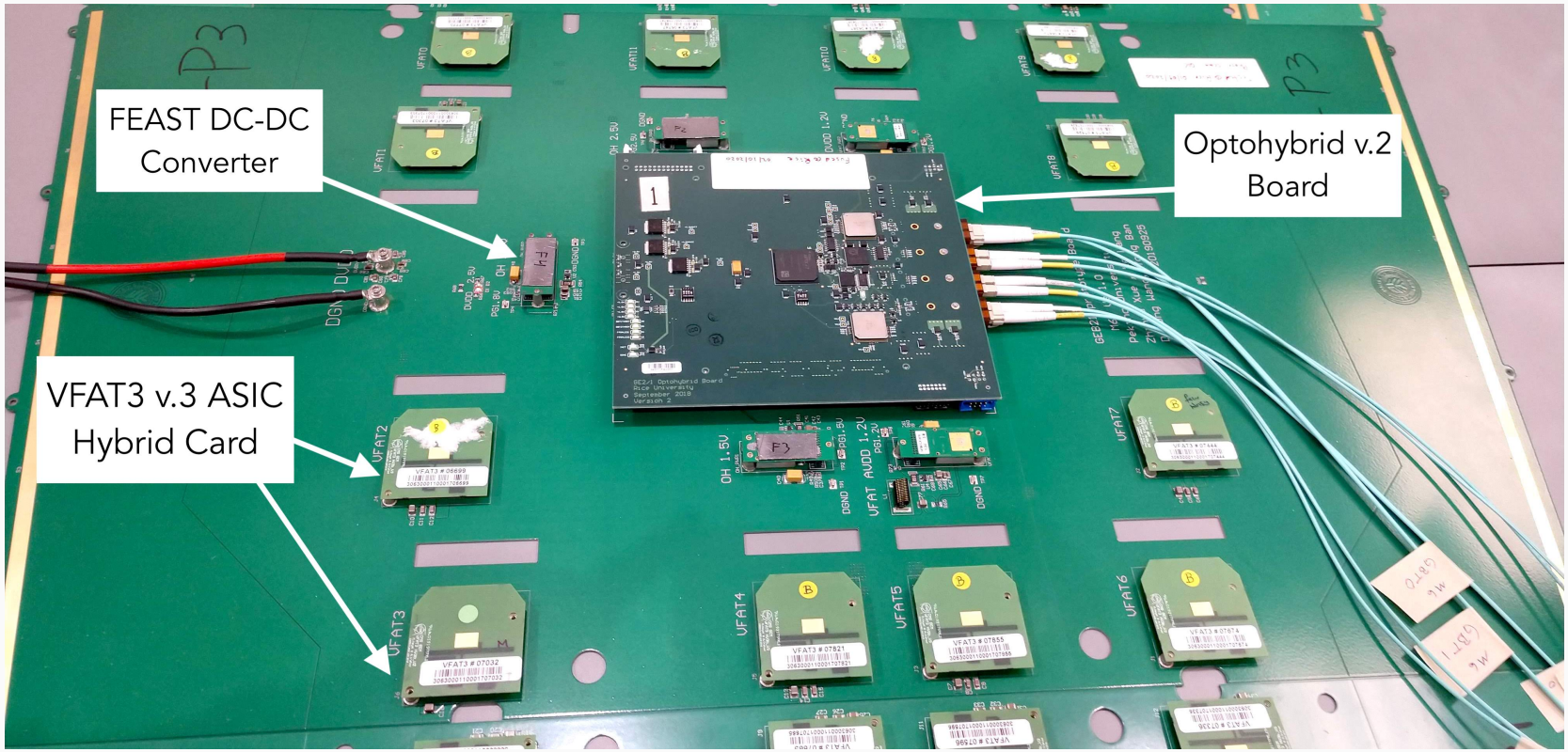
Schematic of the GE2/1 detector [1].



First fully assembled GE2/1 chamber [2].

GE2/1 Electronics Integration

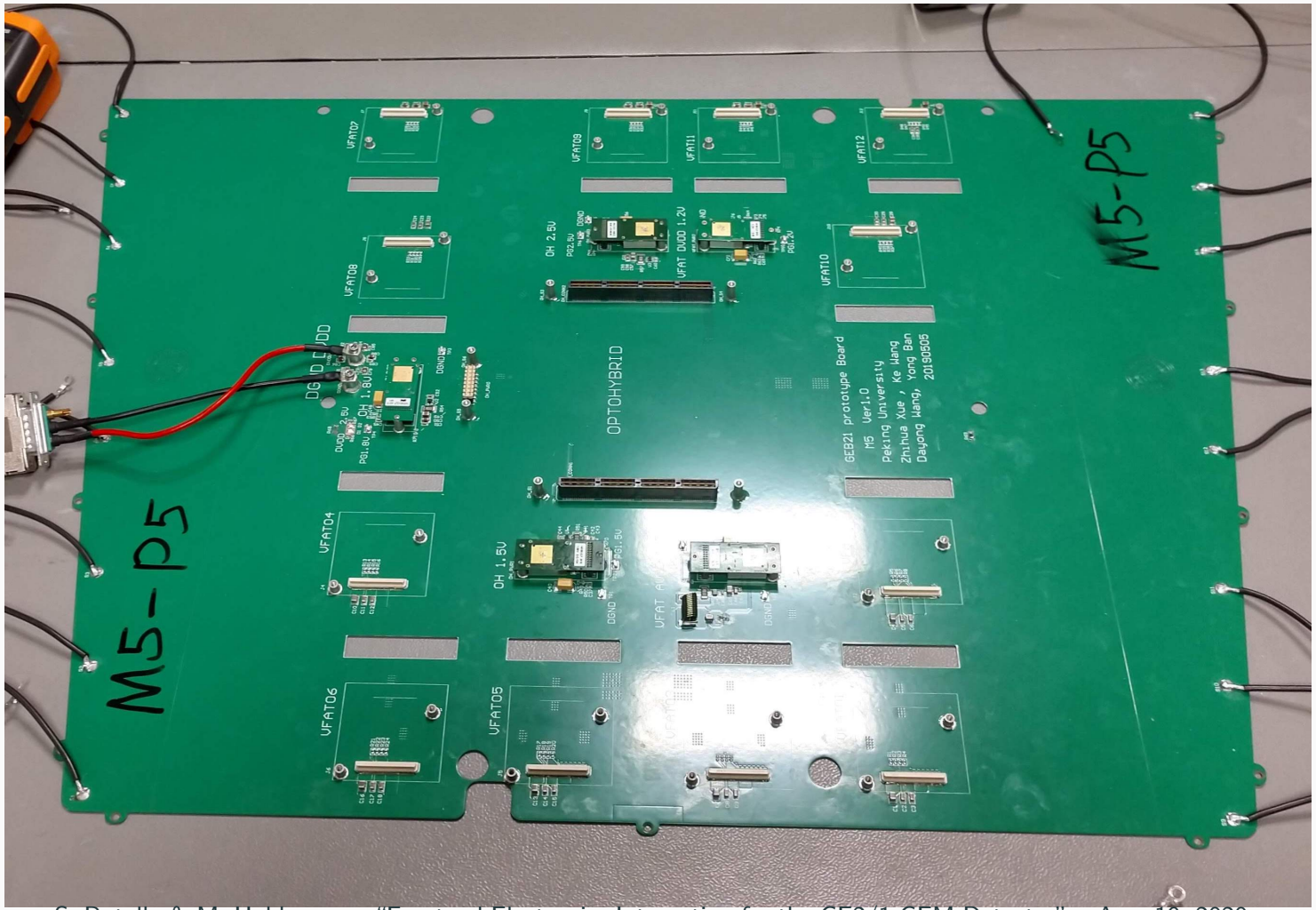
- Before qualifying a chamber for installation in CMS, a chamber needs to have the frontend electronics integrated and calibrated
- This talk will review the frontend electronics on the GE2/1 GEM detector and also the frontend electronics integration procedure



Frontend electronics for the M6 module of the GE2/1 GEM detector.

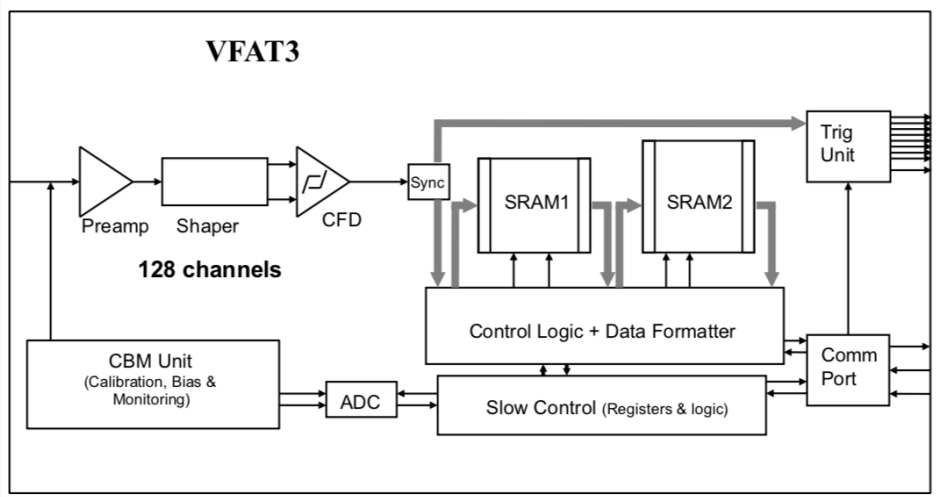
GE2/1 Frontend Electronics Components: GEB

- GEM Electronics Board (GEB)
- The base for all of the frontend electronics
- Routes signals from frontend amplifiers to the optohybrid (OH)
- Secured to the readout board (ROB) of a GE2/1 module

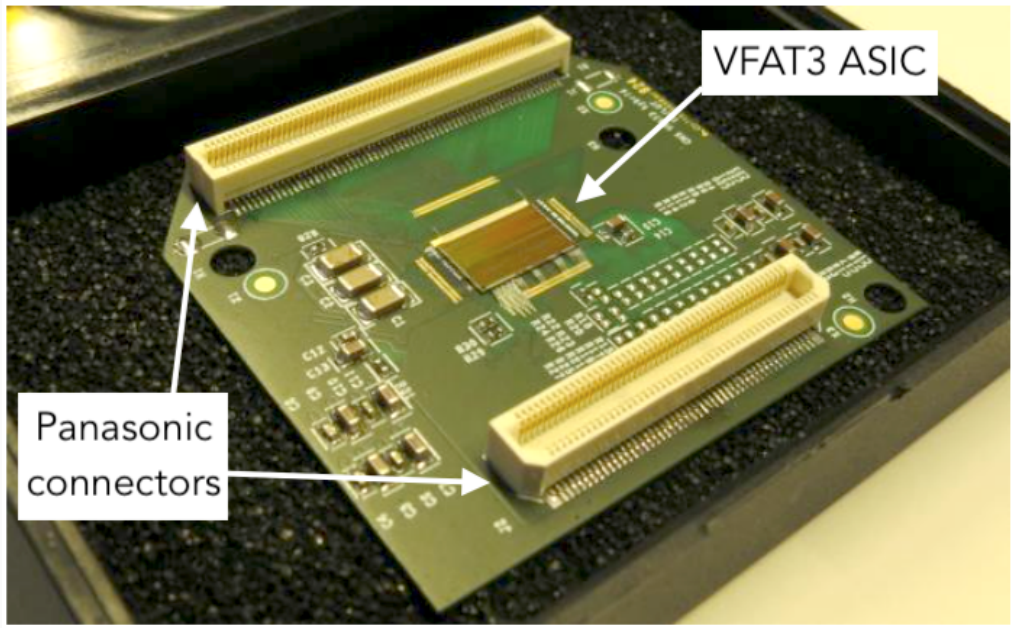


GE2/1 Frontend Electronics Components: VFAT3 Hybrid Card

- (12) ASIC Hybrid Card: Very Forward ATLAS and TOTEM (VFAT3) [3]
- 128 channels, each with an integrating/shaping circuit
- Calibration, bias, and monitoring (CBM) circuit to ensure uniform response for all channels
- Integrates and processes the signal induced on the readout strips
- Binary output: signal above/below threshold



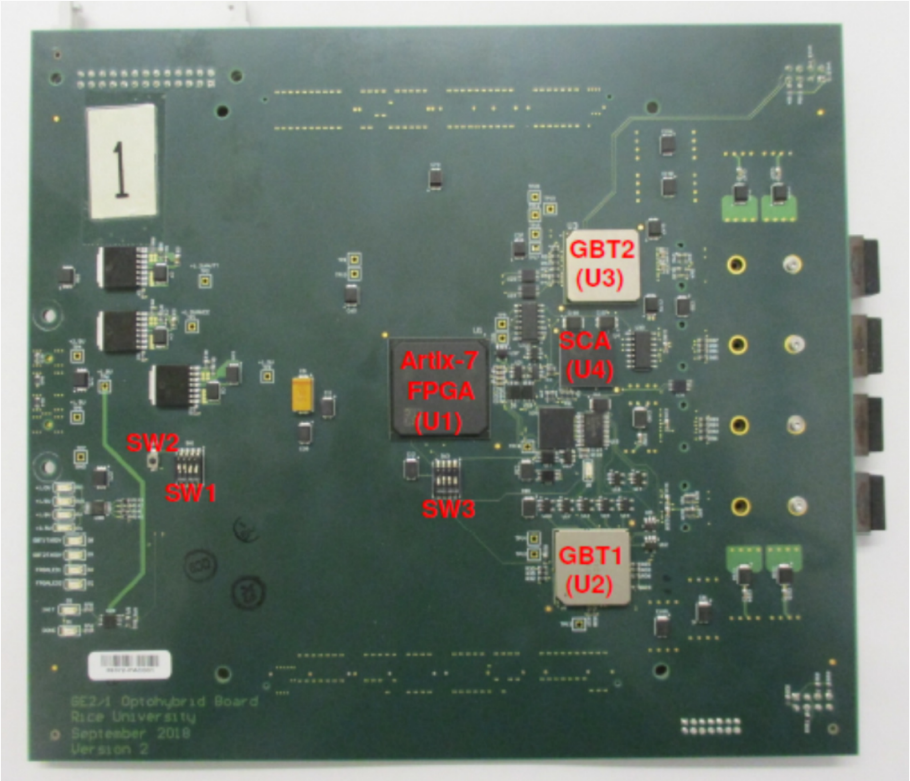
VFAT3 block diagram [3].



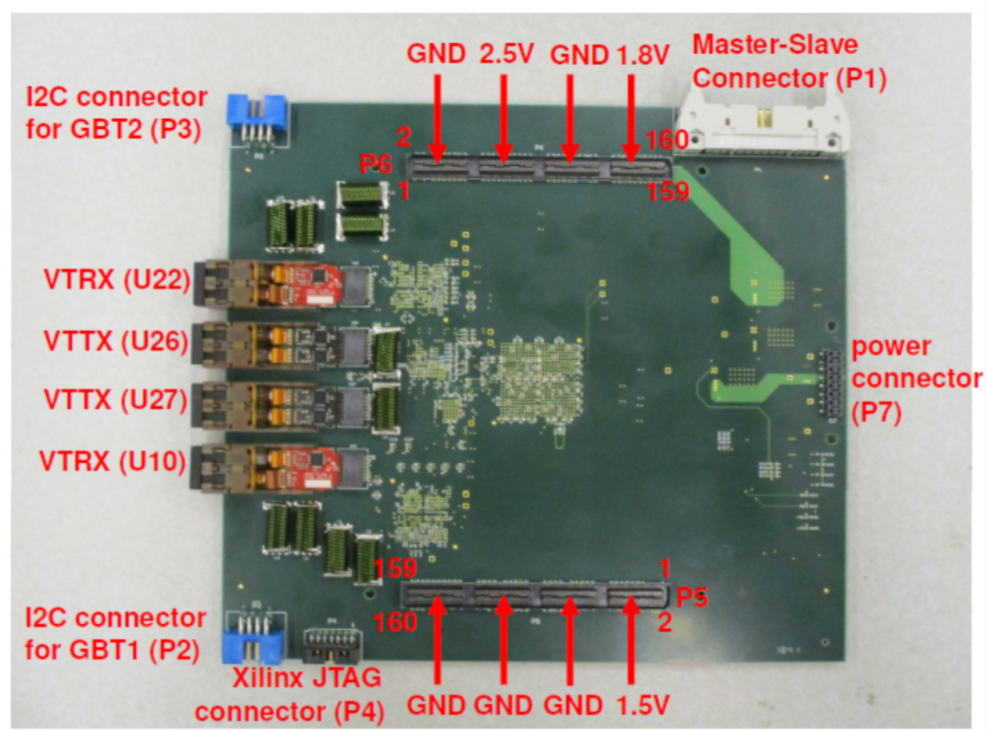
VFAT3 Hybrid Card [3].

GE2/1 Frontend Electronics Components: Optohybrid

- Optohybrid (OH) board [4]
- 1 Artix-7 FPGA [5], 2 Gigabit Transceiver (GBT) ASICs [6], 1 GBT-Slow Control Adapter (SCA) ASIC [7], 4 optical transceivers
- Receives binary signals from VFATs, formats data, sends digital data to DAQ and L1 trigger



Top-side of the OH [4].

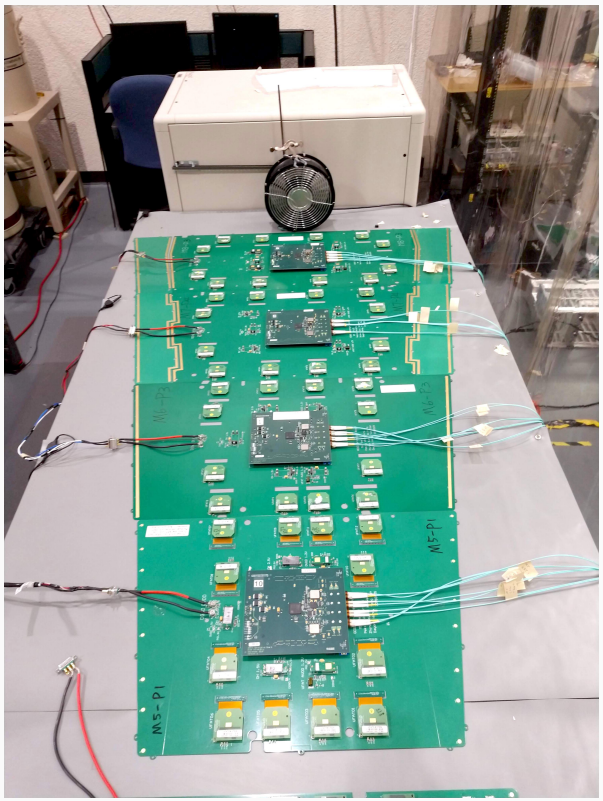


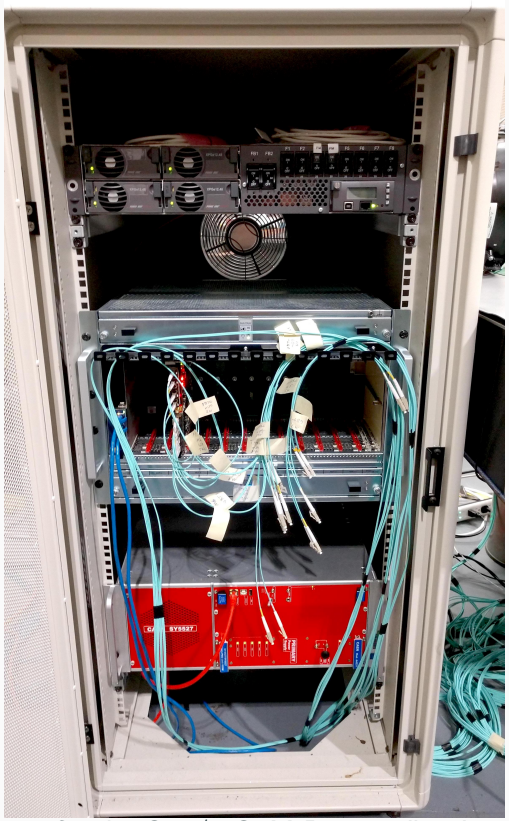
Under-side of the OH [4].

GE2/1 Frontend Electronics Test Stand Setup

- Each GEB and the frontend electronics need to be tested to ensure nominal operation and reliable performance
- GE2/1 electronics integration test stands are located at CERN and Florida Tech
- The test stand at Florida Tech is equipped with the M5-M8 modules of the GE2/1
- DAQ PC/frontend electronics interface utilizes the Gigabit Link Interface Board (GLIB) backend advanced mezzanine card (AMC) in a μTCA architecture

GE2/1 electronics integration test stand at Florida Tech.





Rack with CAEN A1515 power supply, μTCA crate, and GLIB AMC.

GE2/1 Frontend Electronics Integration: VFAT Calibration Values

- Before performing the testing routine ("connectivity" script), calibration data from the VFAT production quality control testing are retrieved from the CMS GEM database (DB) and written to the VFAT configuration files
- A script reads the VFAT chip ID register on a particular GEB and performs DB queries for calibration info for the global registers
- Three configuration files are written with the following parameters:
  - Reference current (`IREF`) values for the reference current for the digital-to-analog (DAC) converter after the bandgap circuit in the CBM unit (used to generate reference currents for all programmable DACs)
  - Analog-to-digital (ADC) reference values for `ADC0` and `ADC1` in the CBM unit (these ADCs are used to monitor all references)
  - DAC calibration values (`cal_DAC`; used for calibrating the calibration pulse circuit)

GE2/1 Frontend Electronics Integration: Connectivity Testing

- The all-in-one script `testConnectivity.py` [9] performs the connectivity testing routine, with the following procedure:
  1. Establish communication with the GBTs
  2. Establish communication with the SCA
  3. Program the FPGA and determine the trigger link status (GEM and CSC trigger)
  4. Perform GBT phase scans and assign correct phases to each VFAT
  5. Check VFAT synchronization

GE2/1 Frontend Electronics Integration: Connectivity Testing

```
====================
Step 4: Checking VFAT Communication
====================
Checking GBT Communication (After Programming FPGA)
GBT Communication Is Stil Good
Scanning GBT Phases, this may take a moment please be patient
====================
Phase Scan Results for OH0
====================
```

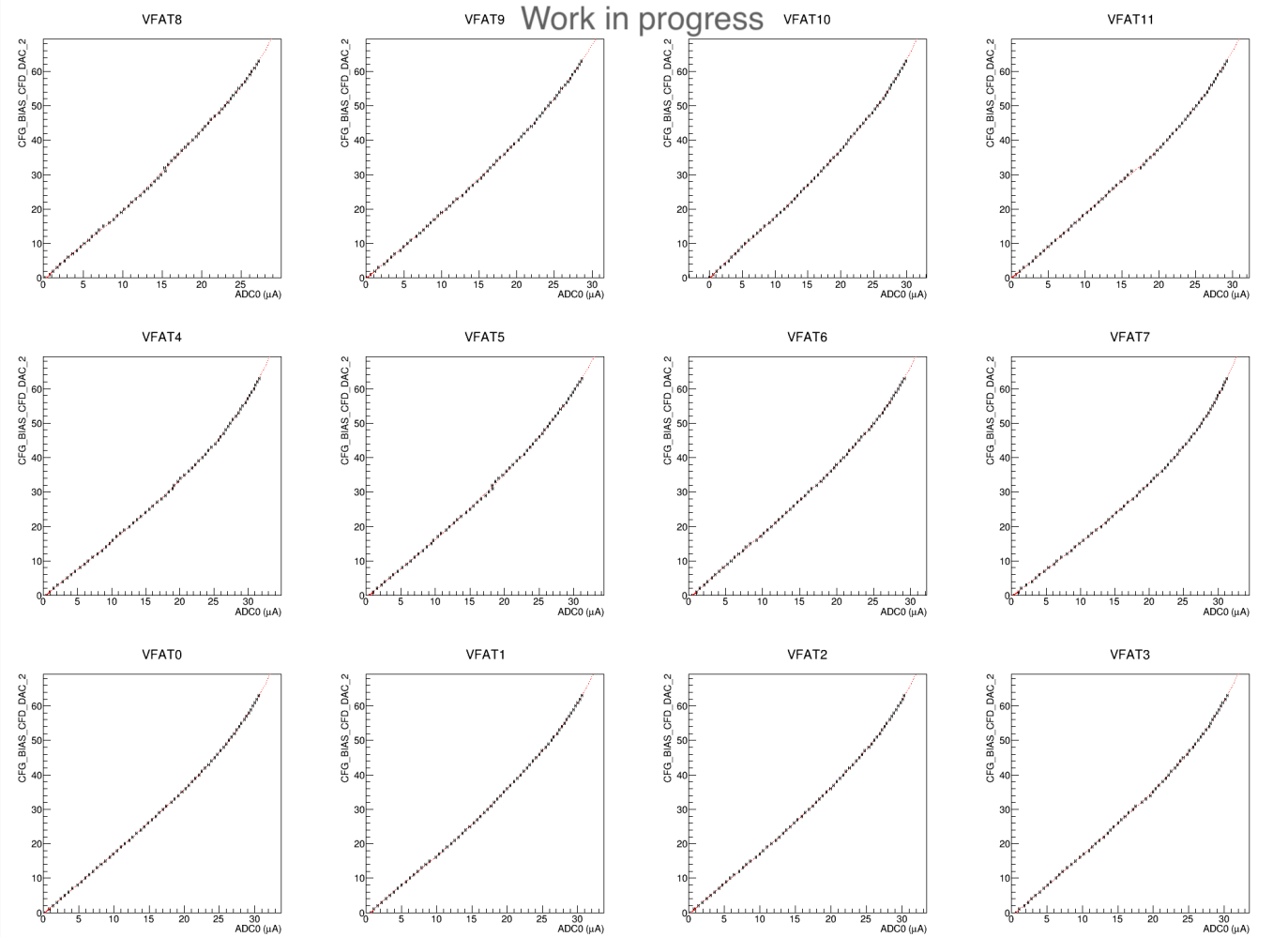
Phase	VFAT0	VFAT1	VFAT2	VFAT3	VFAT4	VFAT5	VFAT6	VFAT7	VFAT8	VFAT9	VFAT10	VFAT11
0	50	50	50	50	50	50	50	50	0	50	50	50
1	50	50	0	50	0	50	50	50	50	50	50	50
2	50	50	50	50	50	50	50	50	50	50	0	50
3	50	50	50	50	50	50	50	50	50	50	50	50
4	50	50	50	50	50	50	0	49	50	50	50	50
5	50	50	50	46	50	50	50	50	50	0	50	50
6	50	50	50	50	50	50	50	50	50	50	50	50
7	0	50	50	50	50	50	50	50	0	50	50	50
8	50	50	50	50	50	0	50	50	50	50	50	50
9	50	50	50	50	0	50	50	50	50	50	50	50
10	50	50	50	50	50	50	50	50	50	50	0	50
11	50	50	50	50	50	50	50	50	50	50	50	50
12	50	50	50	50	50	50	50	50	50	50	50	50
13	50	50	50	50	50	50	50	50	50	0	50	50
14	50	50	50	50	50	50	50	50	50	50	50	50
15	0	0	0	0	0	0	0	0	0	0	0	0

```
Phase 11 will be used for (OH0,VFAT0)
Phase 0 will be used for (OH0,VFAT1)
Phase 5 will be used for (OH0,VFAT2)
Phase 9 will be used for (OH0,VFAT3)
Phase 5 will be used for (OH0,VFAT4)
Phase 12 will be used for (OH0,VFAT5)
Phase 8 will be used for (OH0,VFAT6)
Phase 8 will be used for (OH0,VFAT7)
Phase 4 will be used for (OH0,VFAT8)
Phase 9 will be used for (OH0,VFAT9)
Phase 6 will be used for (OH0,VFAT10)
Phase 0 will be used for (OH0,VFAT11)
Writing Found Phases to frontend
GBT Phases Successfully Writtent to Frontend
03 Apr 2020 05:24:07.882 [7f57e9806740] INFO - utils::_init_num_threads <> - NumExpr defaulting to 4 threads.
====================
```

Example output of the GBT phase scan.

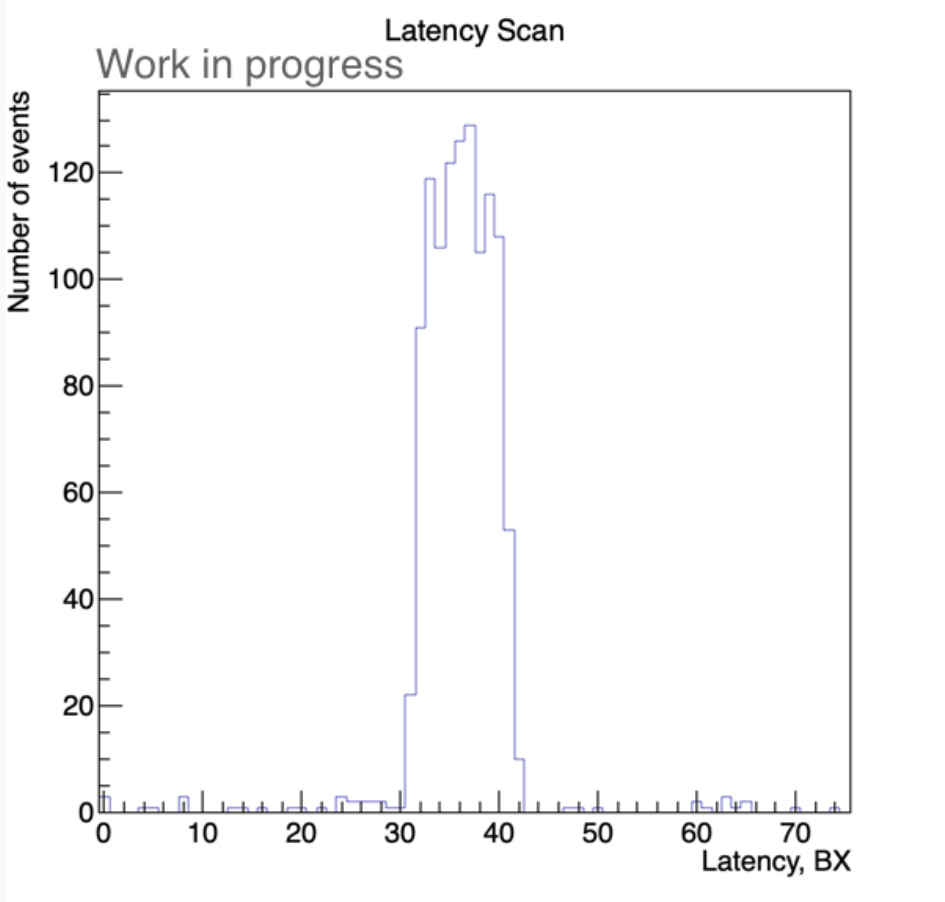
GE2/1 Frontend Electronics Integration: DAC Scans

- DAC scans are performed in-situ for the remaining bias currents/voltages
- Analysis of the DAC scans produces summary plots for each register scanned, and records the nominal DAC values for each VFAT in a calibration file
- Example output for DAC 2 of the constant fraction discriminator (CFD) (DAC register value vs. ADC0 bias current):



GE2/1 Frontend Electronics Integration: Latency Scans

- When the chambers are installed in CMS, the length of the fibers that transmit the L1A trigger signals are not negligible
- The proper latency needs to be determined so that the correct data are sent when an L1A trigger is received
- During a latency scan, trigger signals are sent to the chamber and the total number of hits for each latency value is recorded
- The latency is then determined from the distribution; the bin with the most hits corresponds to the latency chosen for the detector



Latency scan from [10].

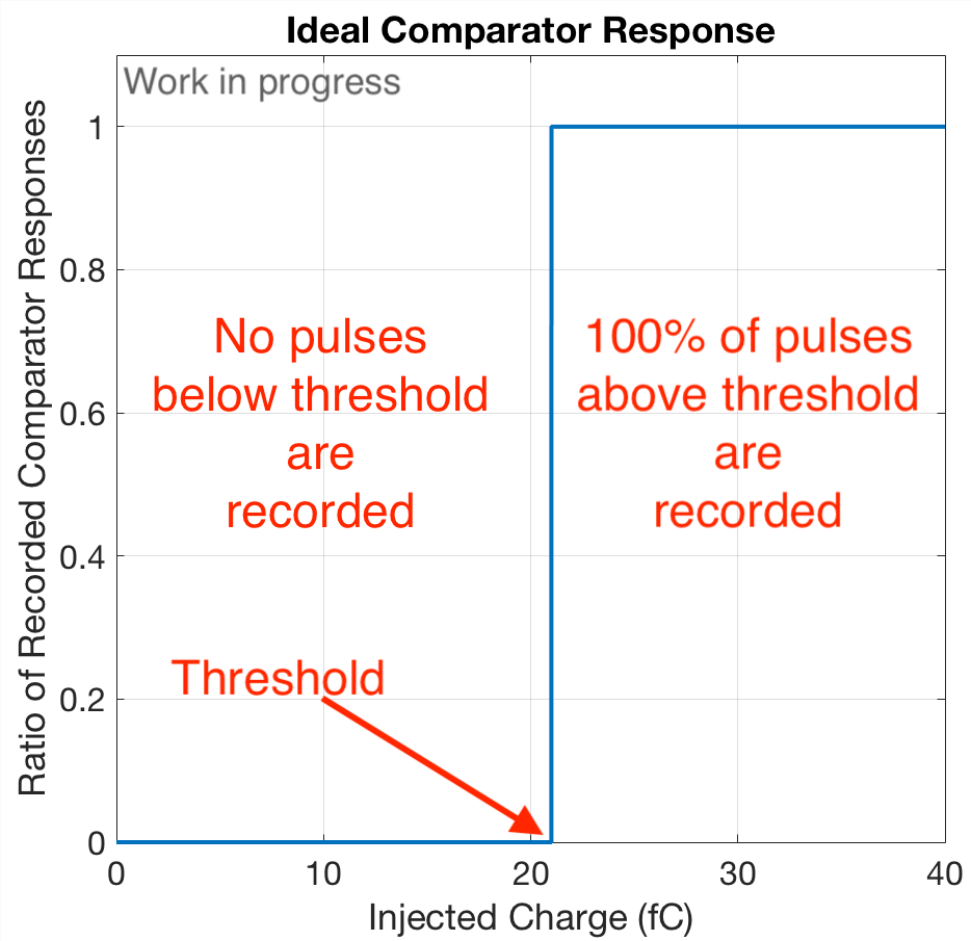
GE2/1 Frontend Electronics Integration: S-curves

- Noise characterization and its reduction is critical to accurate and reliable operation
- One way to determine the noise in the detector/electronics system is to measure the equivalent noise charge (ENC), which is the noise present in the detector preamplifier/amplifier combination
- An S-curve measurement consists of injecting a calibration pulse into one channel of a VFAT and recording how the voltage comparator (0,1) responds at a given threshold
- In an ideal world, the voltage comparator should only respond when the injected charge is greater than the threshold (step function)
- Because there is noise, the actual behavior of the comparator is like a sigmoid function
- The sigma from the fit of a modified error function to the comparator response therefore gives the value of the ENC [11]

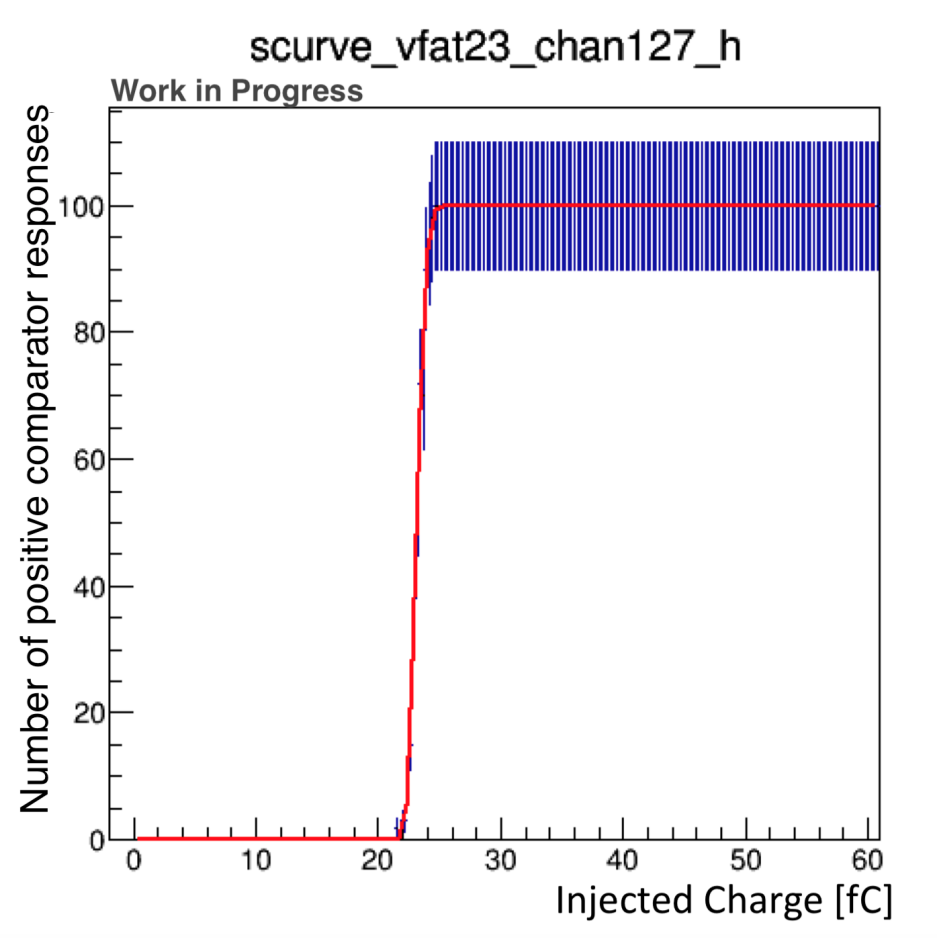
$$f(q) = A\,\mathrm{erf}\left(\frac{\max(P,q)-\mu}{\sqrt{2}\sigma}\right) + A$$

where $A = \frac{n_{inj}}{2}$, n_{inj} is the number of injected charges, q is the injected charge, P is the pedestal value (number of hits with no injected charge), μ is the threshold, σ is the ENC

GE2/1 Frontend Electronics Integration: S-curves

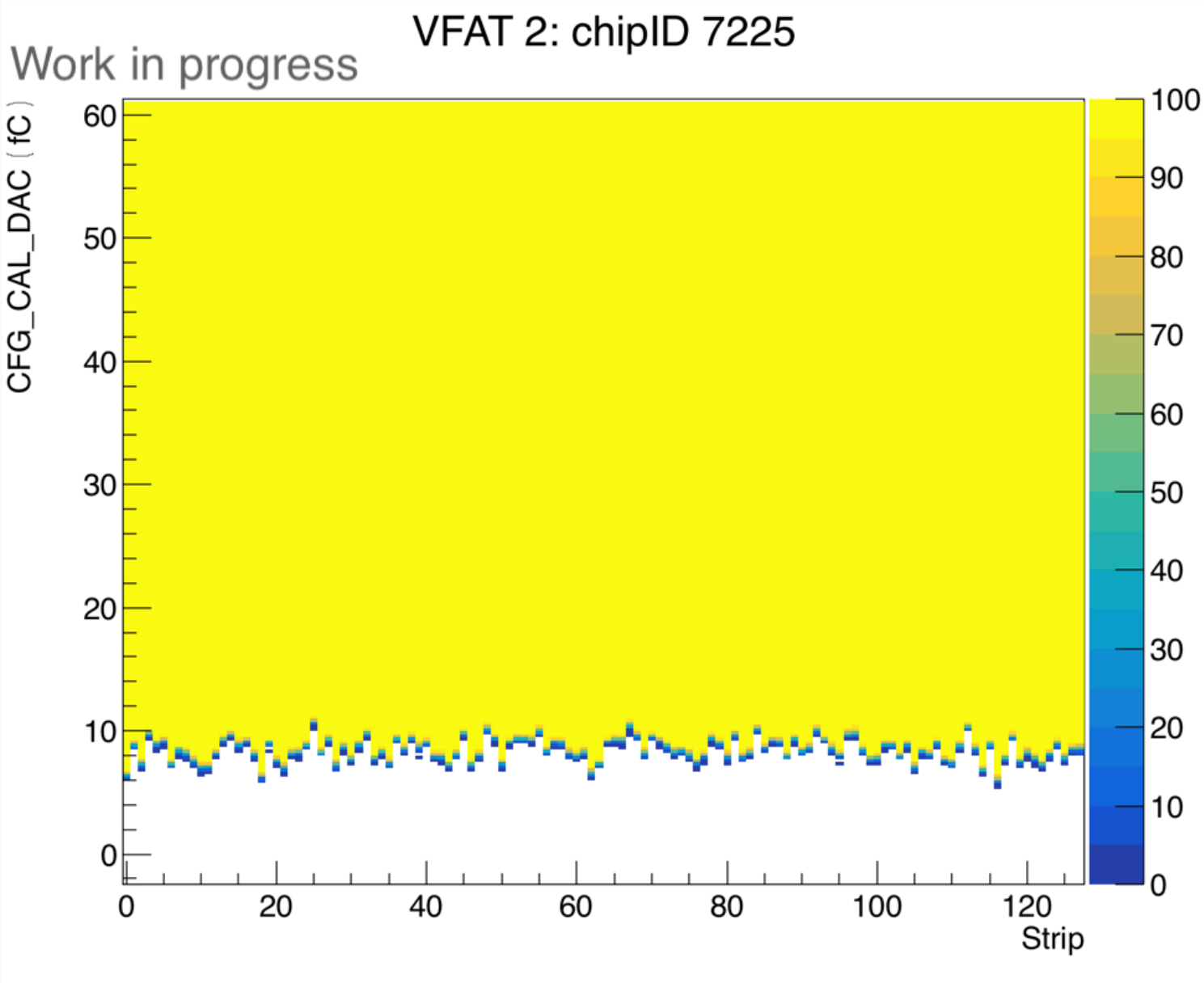


Ideal comparator operation.



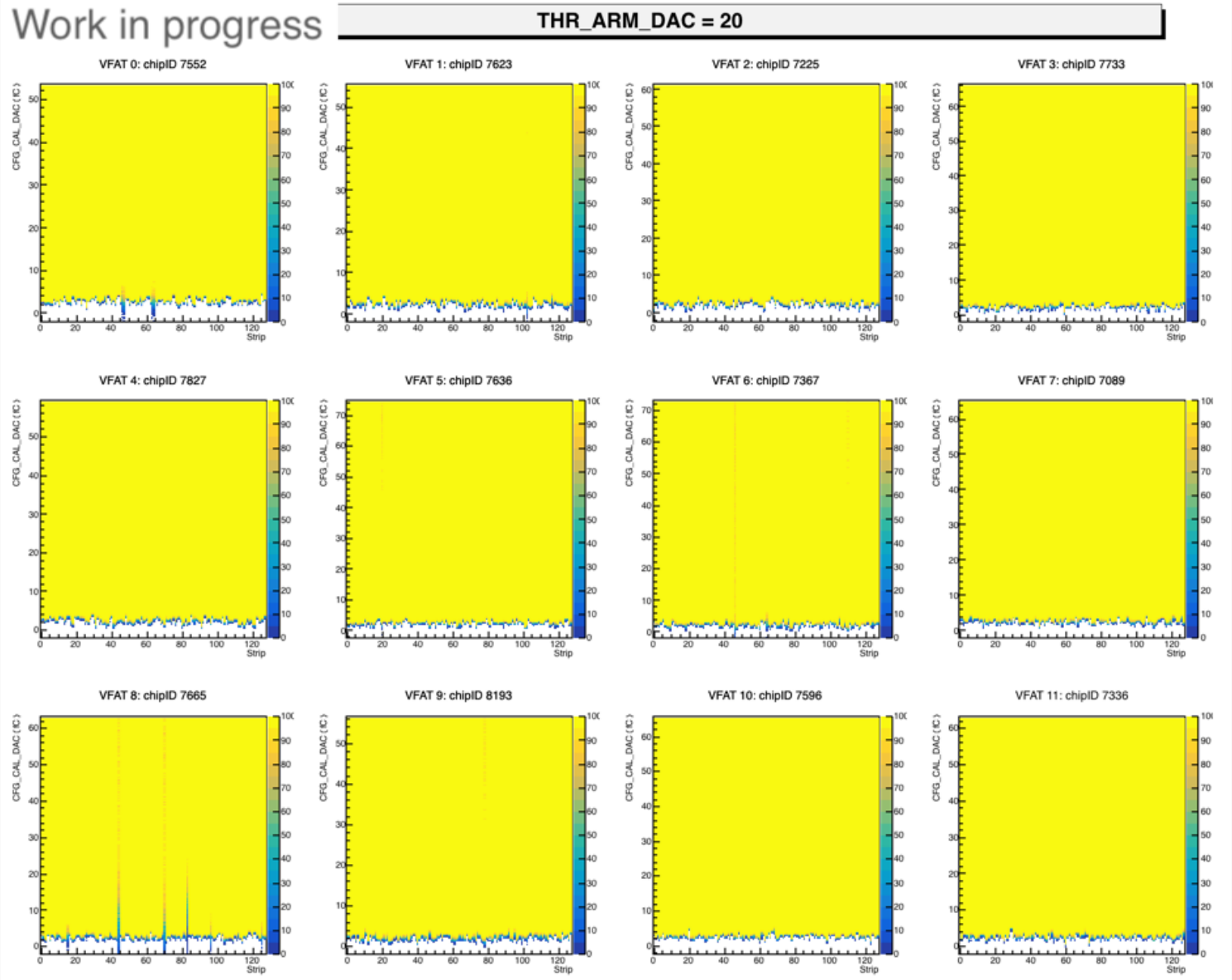
Typical S-curve measurement for one VFAT channel (modified from [11]).

GE2/1 Frontend Electronics Integration: S-curves



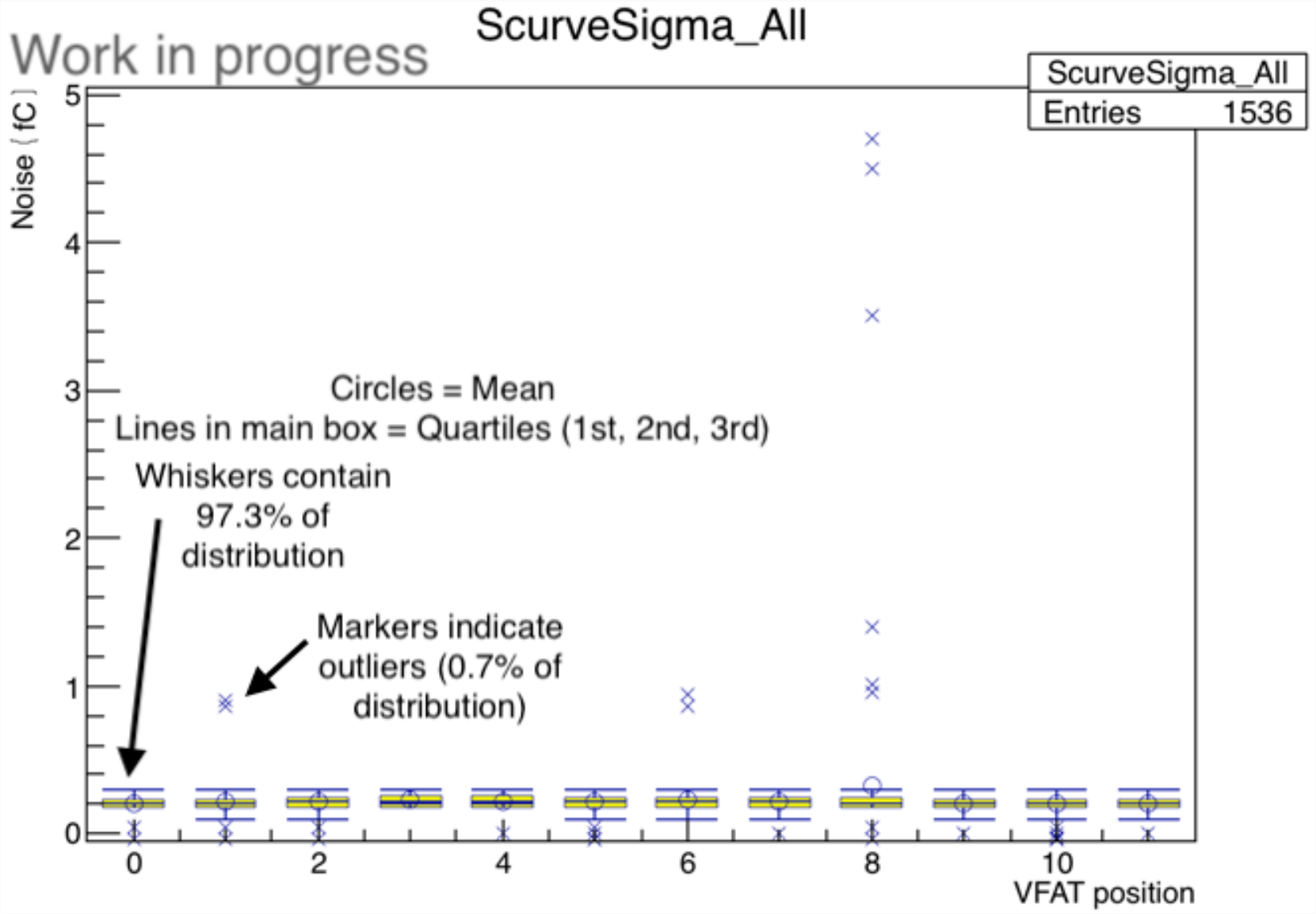
S-curve summary plot showing S-curves for all channels of one VFAT.

GE2/1 Frontend Electronics Integration: S-curves



Scurve summary plot (2D histograms) showing the S-curve of each channel of each VFAT on the GE2/1 module ($12 \cdot 128 = 1536$ channels).

GE2/1 Frontend Electronics Integration: S-curves



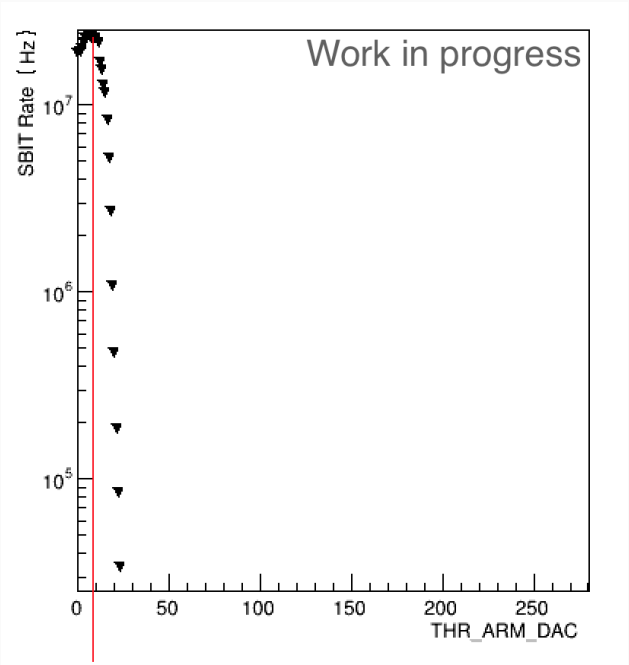
Sigma (ENC) distribution for all channels for each VFAT on one GE2/1 module.

Trigger S-bits

- 128 channels/VFAT, each with an ADC
- All 128 channels are stored in one register of RAM on the VFAT
- L1 trigger sends a signal to the VFAT to send stored data
- The latency and bandwidth set a limit on how much data can be sent/received
- We define a trigger **S-bit** as the binary value of a hit (binary 0 or 1)
- 64 S-bit channels per VFAT (128 channels/2), so two strips worth of information are sent in one S-bit
- These S-bits are multiplexed in time (8 different channels); inputs are taken from the 64 channels, aligned in time, and then sent to the backend electronics
- Note that these trigger S-bits are different than tracking data; these data are transmitted for every bunch crossing (fixed latency) over a different data path than the tracking data

GE2/1 Test Stand: S-bit Threshold Scan

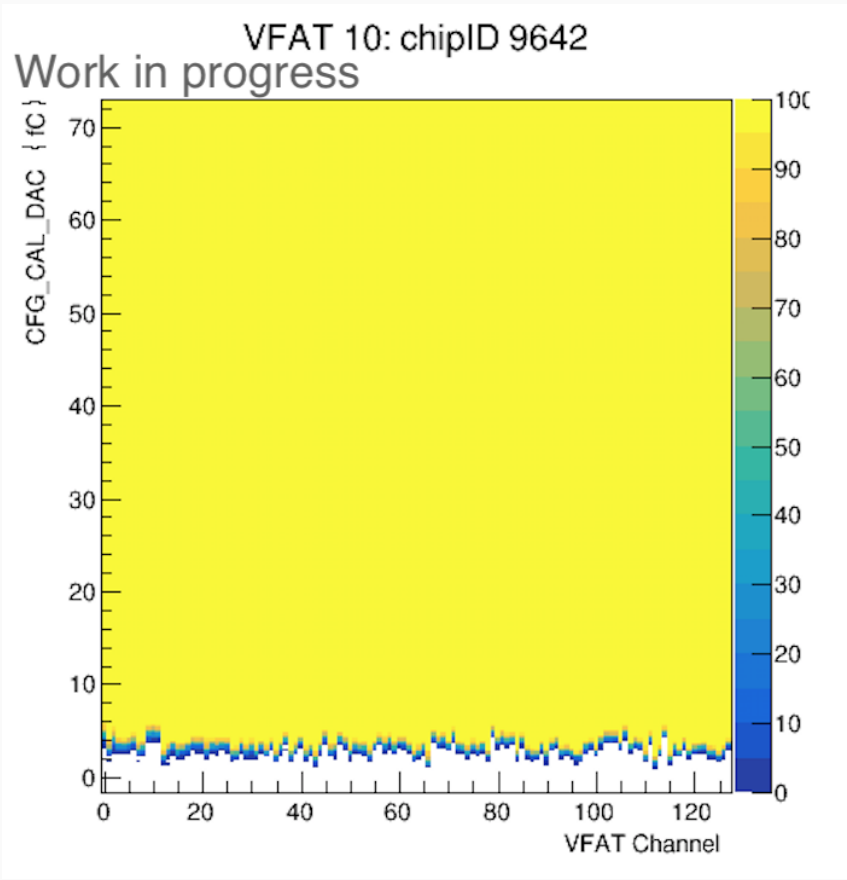
- S-bits are scanned for all VFATs over the DAC comparator threshold (between 0 and 255 DAC units)
- If an S-bit is seen at a particular threshold, it is recorded as a hit
- S-bits are logically OR'ed before recording a hit since all channels are being readout; if all channels fire simultaneously, only one "hit" is recorded for that instant in time
- A profile of the noise in the system is then obtained for all threshold values
- This scan determines the proper threshold of the DAC comparator for an acceptable noise limit (i.e., noise under 1 kHz)



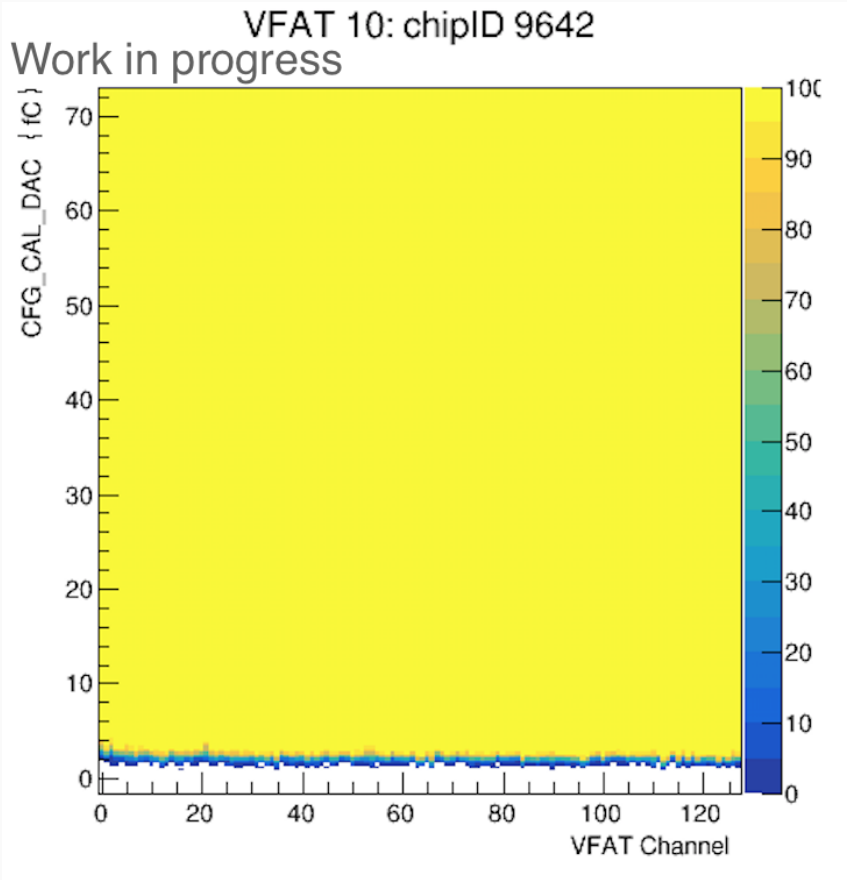
Example S-bit threshold scan for GE1/1 chamber [13].

GE2/1 Test Stand: Trimming

- Scurve means are used in conjunction with Sbit threshold data to add appropriate offsets to each channel threshold of each VFAT on a chamber
- These offsets ensure that all channels respond uniformly to a signal
- Trimming examples shown below for the GE1/1 GEM detector (still to be implemented in GE2/1 chambers)



Before trimming procedure [12].



After trimming procedure [12].

GE2/1 Electronics Integration Status

- Two electronics integration test stands at CERN and FIT
- OH and related firmware development test stands located at Rice and UCLA
- OH Boards
  - 10 OHv1 boards produced (CERN: 4, FIT: 4, UCLA: 1, ULB: 1)
  - 3 OHv2 boards produced (CERN: 1, Rice: 2); 10 to be built in total
- 32 v1 GEBs produced, v2 of GEBs to begin production soon
- 1 GE2/1 back chamber (M1-M4 modules) and 1 GE2/1 front chamber (M5-M8 modules) prototype chambers constructed (one M5 module to be built at FIT)
- Comprehensive noise measurements have been made at CERN and have helped to refine the GEB design for future prototypes [14, 15]
- All CMS GEM DAQ Project software [16] is now compatible with GE2/1 chambers
- Firmware for GE2/1 optohybrids is fully developed and functional

GE2/1 Electronics Integration Summary and Conclusion

- This talk presented an overview of the frontend electronics for the CMS GE2/1 GEM detector, and the connectivity testing and calibration procedure
- As the GE2/1 detector was recently approved for mass production, it is important that the frontend electronics integrate seamlessly into the detector system and function uniformly and accurately
- The following procedures have been successfully implemented for GE2/1 so far:
  1. Establishing connectivity:
     - 1.1 Establish communication with the GBTs
     - 1.2 Establish communication with the SCA
     - 1.3 Program the FPGA and determine the trigger link status (GEM and CSC trigger)
     - 1.4 Perform GBT phase scans and assign correct phases to each VFAT
     - 1.5 Check VFAT synchronization
  2. DAC scans
  3. Latency scans
  4. S-curve measurements
  5. S-bit rate measurements

  Trimming still to be implemented in GE2/1 chambers

Acknowledgements

- We would like to thank Laurent Pétré for his help with the setup of the test stand at FIT and for sharing his knowledge of the software, firmware, and hardware of CMS GEM DAQ operations, Francesco Licciulli for his enlightening insights on the VFAT3 hybrid card, and Mykhailo Dalchenko for sharing his knowledge and experience with the GE2/1 electronics integration setup at CERN

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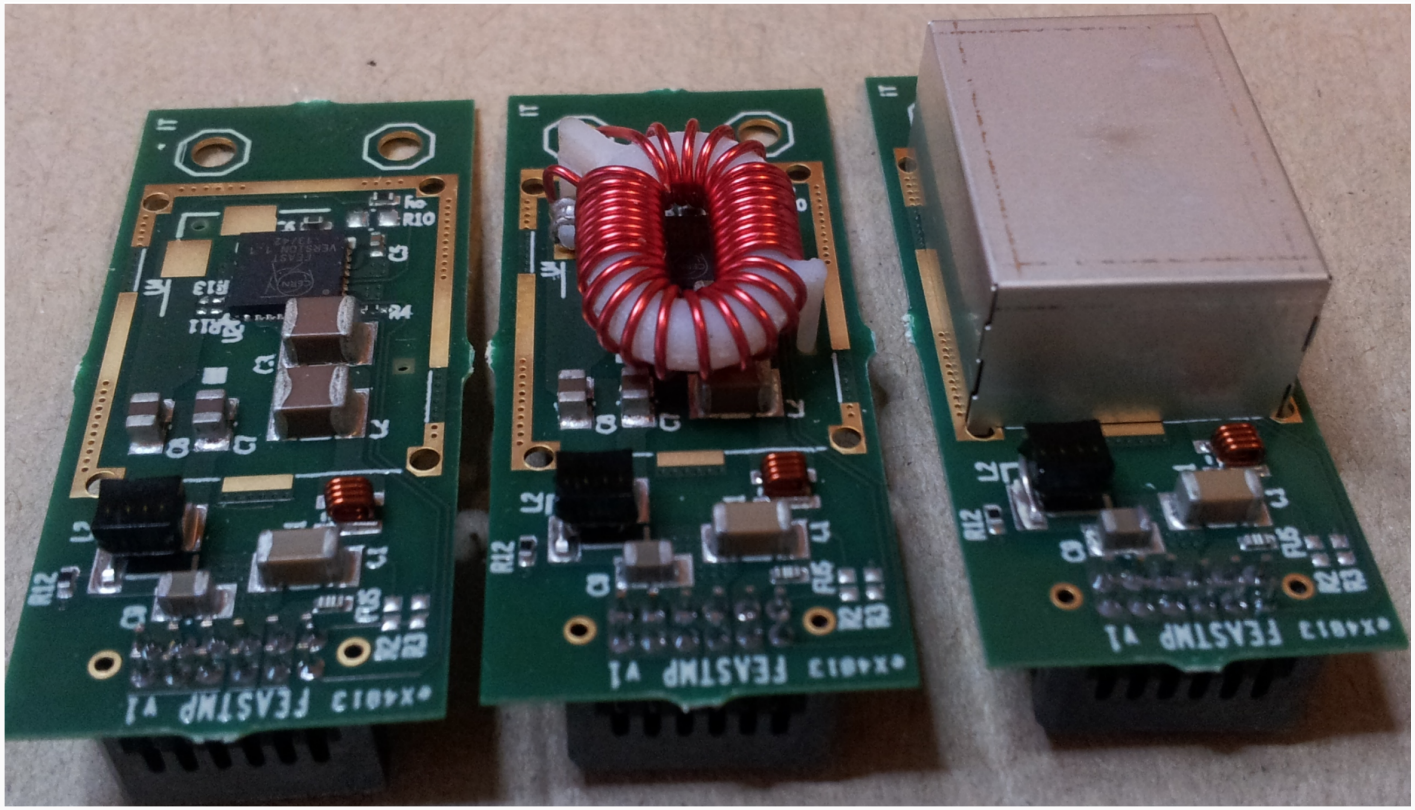
Backup

GE2/1 Frontend Electronics Components: FEAST

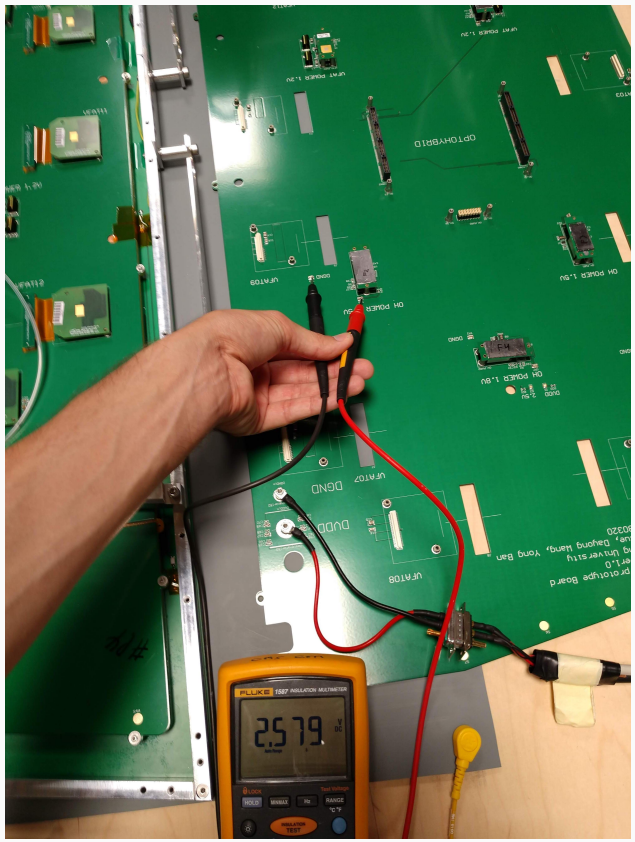
- FEASTMP (FEAST) DC-DC converters
- Total of 5 FEASTs per GE2/1 GEB: (2) 1.2 V, (1) 1.5 V, (1) 1.8 V, (1) 2.5 V
- 1.2 V FEASTs provide power to the VFAT3 hybrids
- 1.5, 1.8, 2.5 V FEASTs provide power to the OH



Picture of the FEAST with the shielding and it's main inductor removed [8].

GE2/1 Frontend Electronics Integration Procedure

- Before adding the frontend electronics to the GEB, low voltage (LV) distribution by the FEASTs need to be tested to ensure nominal operating voltage for all electronics
- A multimeter is used at 5 test points on the GEB to test each FEAST



Testing FEAST voltages.

Table 1: Voltage Tolerance of the FEASTs

Nominal Voltage (V)	Tolerance Range (V)
1.20	[1.17, 1.27]
1.55	[1.47, 1.59]
1.86	[1.76, 1.91]
2.58	[2.45, 2.66]

GE2/1 Frontend Electronics Integration: DAC Scans

- DAC scans are performed in-situ for the remaining bias currents/voltages

Table 2: Bias-Programmable Registers Optimized During the DAC Scan

Register	Description
CFD_Bias1	CFD bias current 1
CFD_Bias2	CFD bias current 2
CFD_Hyst	Hysteresis DAC bias current
CFG_BIAS_PRE_I_BIT	Preamplifier bias input transistor bias current
CFG_BIAS_PRE_I_BSF	Preamplifier bias source follower bias current
CFG_BIAS_PRE_I_BLCC	Preamplifier bias leakage compensation bias current
CFG_BIAS_PRE_VREF	Preamplifier reference voltage
CFG_BIAS_SH_I_BFCAS	Shaper folded cascode bias current
CFG_BIAS_SH_I_BDIFF	Shaper input pair bias current
CFG_BIAS_SD_I_BDIFF	SD input pair bias current
CFG_BIAS_SD_I_BFCAS	SD folded cascode bias current
CFG_BIAS_SD_I_BSF	SD source follower bias current