Status of SCRIBE

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on behalf of FIT team

Overview

SCRIBE (Slow Control and Run Initialization byte-wise environment) is a new tool being developed/adopted by CMS GEM assembly sites to facilitate FEC configuration, DATE data-taking and AMORE data-analysis during QC5.

SCRIBE in a nutshell
- Cross-platform web-interface, fast learning curve
- Quick and easy FEC/APV25 configuration procedure featuring implementation of ZS
- Firmware Pedestal monitoring
- Supports all FEC versions w/o ZS (*SCRIBE version >=2*)*
- RPM installation user-indipendent (*SCRIBE version >=2.3*)
- Start/stop single/multiple runs featuring latency scan (*SCRIBE version >=2*)
- Near-real time AMORE data-analysis (*SCRIBE version >2=*)
- Multi-nodal: each SCRIBE node can run analysis and/or run DAQ (*SCRIBE version>=2.3*)
  - → parallel data-analysis + DAQ computer hot swap

*Thanks to TAMU the FECv6 firmware now has been built with ZS module, preliminary tests at FIT confirms that such firmware works correctly!

FIT and CERN sites are already profitting of SCRIBE for QC5; *get SCRIBE RPM installed!*

Configuring the SRS

Slow Control & Run Initialization Byte-wise Environment

| General | SRS system | ADC Card | APV Application Registers | APV Hybrid Registers | APZ Registers | ZS PEDESTALS | DAQ |

Settings and Utility tools

Elog
Elog hostname: `localhost`   Elog port: `8080`   User: `Default`   ☐ Automatic Elog [Save values]

Computer
Eth0: 163.118.204.139

Eth1 10.0.0.3

Eth2

Online Monitor/Control

SRS FEC Ports

SRS System Port: `6007`
ADC Card Port: `6519`
APV Application Registers Port: `6039`
APV Hybrid Registers Port: `6263`
APZ Register Port: `6040`

[Initialize SRS]
☑ System ☑ FEC ☑ APV AR ☑ APV H ☐ APZ
[Save SRS]   _____   Message

SRS FECs

Total number of FECs `1`

FEC IP: `10` `0` `0` `2`   FEC number `1`
FEC IP: `10` `0` `9` `2`   FEC number `2`
FEC IP: ___ ___ ___ ___   FEC number `3`
FEC IP: ___ ___ ___ ___   FEC number
FEC IP: ___ ___ ___ ___

[Apply configuration]

["Run 33 stop "]

Elog server settings for time capsule of all values of SRS (executed automatically any user writes any register)

Computer ethernet cards

General settings of SRS

SRS ports (firmware coded)

Total number of FEC in the setup
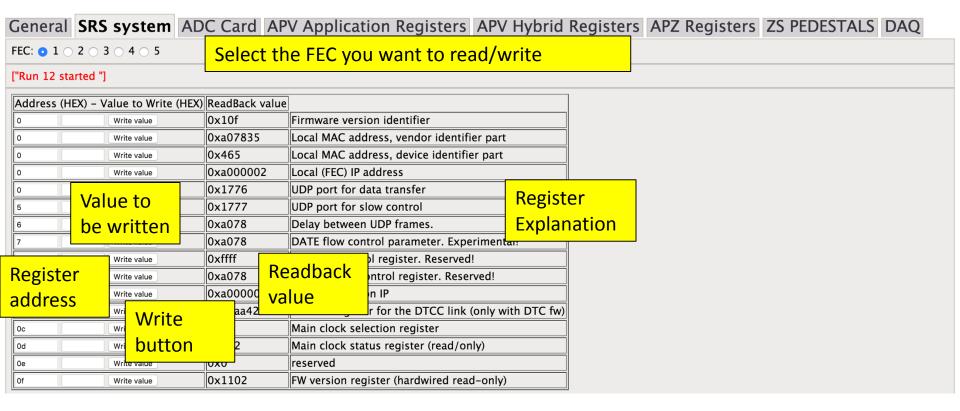
IP of each FEC to be monitored/controlled

INFO MESSAGE: Configuration, data start/stop/SRS writing into registers, reading etc etc (This is shown on all pages so user knows the status/action takes)
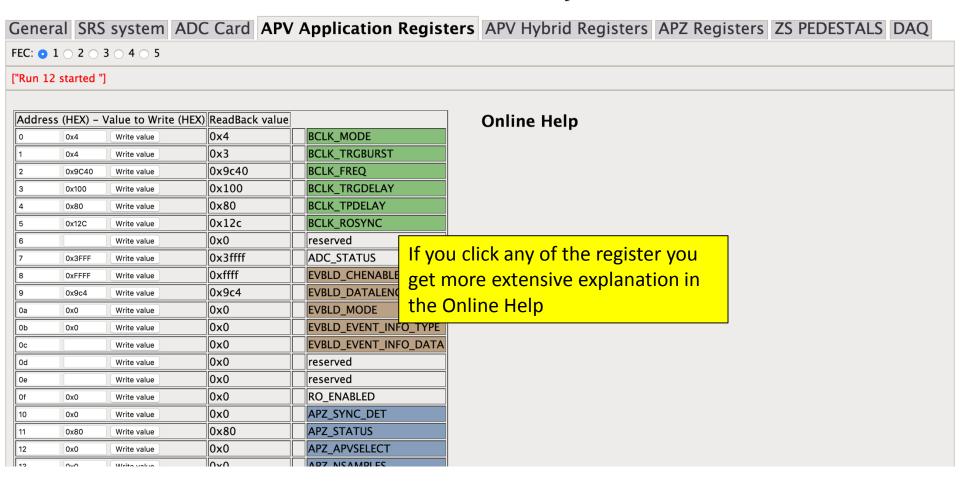
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Configuring the SRS

Slow Control & Run Initialization Byte-wise Environment

| General | **SRS system** | ADC Card | APV Application Registers | APV Hybrid Registers | APZ Registers | ZS PEDESTALS | DAQ |

FEC: ⦿ 1 ○ 2 ○ 3 ○ 4 ○ 5

Select the FEC you want to read/write

["Run 12 started "]

Address (HEX) – Value to Write (HEX)	ReadBack value	
0 [Write value]	0x10f	Firmware version identifier
0 [Write value]	0xa07835	Local MAC address, vendor identifier part
0 [Write value]	0x465	Local MAC address, device identifier part
0 [Write value]	0xa000002	Local (FEC) IP address
0	0x1776	UDP port for data transfer
5	0x1777	UDP port for slow control
6	0xa078	Delay between UDP frames.
7	0xa078	DATE flow control parameter. Experimental
[Write value]	0xffff	ol register. Reserved!
[Write value]	0xa078	ntrol register. Reserved!
[Write value]	0xa00000	n IP
Wr...aa42		r for the DTCC link (only with DTC fw)
0c Wr		Main clock selection register
0d Wr...2		Main clock status register (read/only)
0e [Write value]	0x0	reserved
0f [Write value]	0x1102	FW version register (hardwired read-only)

Value to be written

Register Explanation

Readback value

Register address

Write button

Configuring the SRS

Slow Control & Run Initialization Byte-wise Environment

General	SRS system	**ADC Card**	APV Application Registers	APV Hybrid Registers	APZ Registers	ZS PEDESTALS	DAQ

FEC: ● 1 ○ 2 ○ 3 ○ 4 ○ 5

["Run 12 started "]

Address (HEX) – Value to Write (HEX)			ReadBack value			
0	0xff	Write value	0x41ff	HYBRID_RST_N	Reset pin for each HDMI channel. Valid low for the APV hybrid.
1	0x0	Write value	0x43ff	PWRDOWN_CH0	Power–down control of the analog circuitry for the master path for each HDMI channel
2	0x0	Write value	0x45ff	PWRDOWN_CH1	Power–down control of the analog circuitry for the slave path for each HDMI channel
3	0x0	Write value	0x47ff	EQ_LEVEL_0	Equalization control (bit 0) for each HDMI channel
4	0x0	Write value	0x49ff	EQ_LEVEL_1	Equalization control (bit 1) for each HDMI channel
5	0x0	Write value	0x4bff	TRGOUT_ENABLE	Enables TRGOUT buffer for each HDMI channel
6	0xff	Write value	0x4dff	BCLK_ENABLE	Enables BCLK buffer for each HDMI channel

Online help

Register Bit	7	6	5	4	3	2	1	0
Corresponding HDMI cable	4	5	6	7	0	1	2	3

Configuring the SRS

Slow Control & Run Initialization Byte-wise Environment

| General | SRS system | ADC Card | **APV Application Registers** | APV Hybrid Registers | APZ Registers | ZS PEDESTALS | DAQ |

FEC: ● 1 ○ 2 ○ 3 ○ 4 ○ 5

["Run 12 started "]

Address (HEX) – Value to Write (HEX)		ReadBack value		
0	0x4	Write value	0x4	BCLK_MODE
1	0x4	Write value	0x3	BCLK_TRGBURST
2	0x9C40	Write value	0x9c40	BCLK_FREQ
3	0x100	Write value	0x100	BCLK_TRGDELAY
4	0x80	Write value	0x80	BCLK_TPDELAY
5	0x12C	Write value	0x12c	BCLK_ROSYNC
6		Write value	0x0	reserved
7	0x3FFF	Write value	0x3ffff	ADC_STATUS
8	0xFFFF	Write value	0xffff	EVBLD_CHENABLE
9	0x9c4	Write value	0x9c4	EVBLD_DATALEN
0a	0x0	Write value	0x0	EVBLD_MODE
0b	0x0	Write value	0x0	EVBLD_EVENT_INFO_TYPE
0c		Write value	0x0	EVBLD_EVENT_INFO_DATA
0d		Write value	0x0	reserved
0e		Write value	0x0	reserved
0f	0x0	Write value	0x0	RO_ENABLED
10	0x0	Write value	0x0	APZ_SYNC_DET
11	0x80	Write value	0x80	APZ_STATUS
12	0x0	Write value	0x0	APZ_APVSELECT
13	0x0	Write value	0x0	APZ_NSAMPLES

Online Help

If you click any of the register you get more extensive explanation in the Online Help

Configuring the SRS

Slow Control & Run Initialization Byte-wise Environment

General	SRS system	ADC Card	APV Application Registers	**APV Hybrid Registers**	APZ Registers	ZS
PEDESTALS	DAQ					

FEC: ◉ 1 ○ 2 ○ 3 ○ 4 ○ 5

HDMI: ◉ 0 ○ 1 ○ 2 ○ 3 ○ 4 ○ 5 ○ 6 ○ 7
APV ◉ Master ○ Slave

["Run 12 started "]

For APV register you should select which HDMI and which chip to r/w (previous ports acted for every FEC)

Address (HEX) – Value to Write (DEC)			ReadBack value	
0		Write value	0x6b00	ERROR
1	19	Write value	0x6b04	MODE
2	128	Write value	0x6b84	LATENCY
3	4	Write value	0x6b04	MUX_GAIN
10	98	Write value	0x6b00	IPRE
11	52	Write value	0x6b00	IPCASC
12	34	Write value	0x6b00	IPSF
13	34	Write value	0x6b00	ISHA
14	34	Write value	0x6b00	ISSF
15	55	Write value	0x6b00	IPSP
16	16	Write value	0x6b00	I_MUX_IN
18	100	Write value	0x6b00	ICAL

Online Help

Configuring the SRS

Slow Control & Run Initialization Byte-wise Environment

General | SRS system | ADC Card | APV Application Registers | APV Hybrid Registers | **APZ Registers** | ZS
PEDESTALS | DAQ

FEC: ◉ 1 ○ 2 ○ 3 ○ 4 ○ 5

HDMI: ◉ 0 ○ 1 ○ 2 ○ 3 ○ 4 ○ 5 ○ 6 ○ 7
APV ◉ Master ○ Slave

["Run 12 started "]

Pedestals

Address		ReadBack value	
0	Write value	--	PED CH0
16	Write value	--	PED CH 1
32	Write value	--	PED CH 2
48	Write value	--	PED CH 3
64	Write value	--	PED CH 4
80	Write value	--	PED CH 5
96	Write value	--	PED CH 6
112	Write value	--	PED CH 7
4	Write value	--	PED CH 8
20	Write value	--	PED CH 9

Sigma

Address		ReadBack value	
80000000	Write value	--	PED CH0
80000016	Write value	--	PED CH 1
80000032	Write value	--	PED CH 2
80000048	Write value	--	PED CH 3
80000064	Write value	--	PED CH 4
80000080	Write value	--	PED CH 5
80000096	Write value	--	PED CH 6
80000112	Write value	--	PED CH 7
80000004	Write value	--	PED CH 8
80000020	Write value	--	PED CH 9
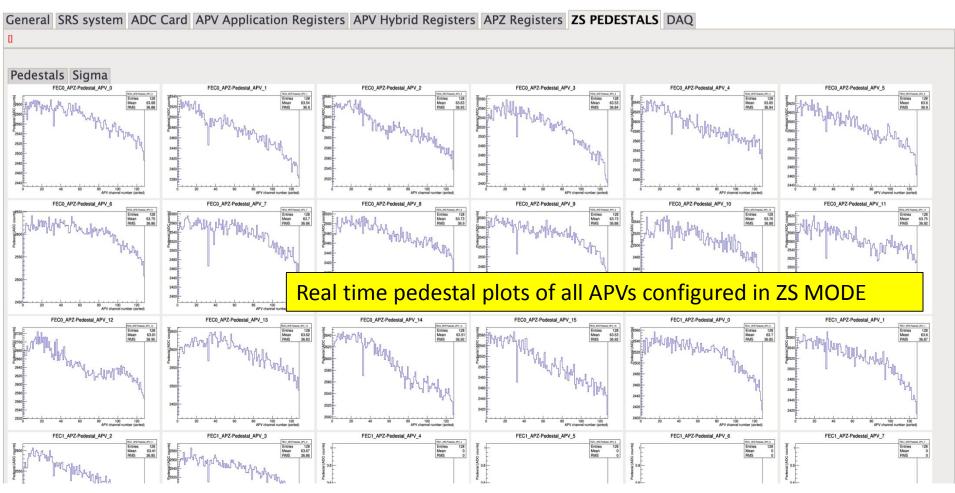
This register holds pedestal data (at firmware level) so output data is zero suppressed,
Here you could mask/unmask any channel on any chip for instance..

Configuring the SRS

Slow Control & Run Initialization Byte-wise Environment

General | SRS system | ADC Card | APV Application Registers | APV Hybrid Registers | APZ Registers | **ZS PEDESTALS** | DAQ

Pedestals | Sigma

Real time pedestal plots of all APVs configured in ZS MODE

Data-taking

Slow Control & Run Initialization Byte-wise Environment

| General | SRS system | ADC Card | APV Application Registers | APV Hybrid Registers | APZ Registers | ZS PEDESTALS | **DAQ** |
| AMORE | DQM |

[]

DAQ CONFIGURATION

["DAQ ACTIVATED"]

Rawdata folder /mnt/nas1/cmsgem
Rawdata filename gemsrs.raw
Number of runs 20
Number of events per run 500000   Update values

Configure ZS

Activate DAQ   Deactivate DAQ
DATE ON   Start run   Stop run   DATE RESET

Start multiple runs   Stop multiple runs
Enable/Disable smart scan ☐
Port ___ Address ___ Start ___ Stop ___
Use HEX instead of DEC ☐

FEC configuration button supports any FEC version

DATE commands (start/stop) for single and/or multiple runs

Smartscan for multiple run while scanning a register (latency)

Data-analysis

Slow Control & Run Initialization Byte-wise Environment

| General | SRS system | ADC Card | APV Application Registers | APV Hybrid Registers | APZ Registers | ZS PEDESTALS | DAQ | **AMORE** | DQM |

["Run 770 finished\n"]

New acknowledgement about activation of automatic AMORE
In case of multiple nodes, any machine can have this activated

AMORE CONFIGURATION

["AUTOMATIC ANALYSIS ACTIVATED"]

Rawdata folder /mnt/nas1/cmsgem

Events per cycle 50000
Cycles 10
Process 1 ☑ Process 2 ☑ Process 3 ☑ Process 4 ☑ Process 5 ☑ Process 6 ☑
[Update AMORE settings]

Any computer node can commit one or more cores to the analysis

Single Run to analyze [   ] offset events 0 [Run on this]
Multiple-merged runs to analyze from [   ] for runs 20 with events 500000 [Run on these]

Event shifter

[Empty run pool] [Activate automatic analysis] [Deactivate automatic analysis]
[Kill process 1] [Kill process 2] [Kill process 3] [Kill process 4] [Kill process 5] [Kill process 6]

New buttons to terminate any AMORE process

RUNS IN POOL

if all cores of all nodes are busy, any run waiting to be analyzed will be queued in this pool

AMORE PROCESS 1

["Launched with : amoreAgent -a SRS01 -s \/mnt\/nas1\/cmsgem\/fitgem973.raw -e 50000 -c 10 \n","setting infologger destination to stdout\n"," SRSConfiguration::Load() ==> RUNTYPE ROOTFILE\n"," SRSConfiguration::Load() ==> RUNNAME \/mnt\/nas1\/cmsgem\/fitgem973\n"," SRSConfiguration::Load() ==> CYCLEWAIT 2\n"," SRSConfiguration::Load() ==> ZEROSUPCUT 10\n"," SRSConfiguration::Load() ==> MINCLUSTSIZE 1\n"," SRSConfiguration::Load() ==> MAXCLUSTSIZE 50\n"," SRSConfiguration::Load() ==> MAXCLUSTMULT 500\n"," SRSConfiguration::Load() ==> HISTCFG \/home\/SRSUser\/amoreSRS\/configFileDir\/histogram_default.cfg\n"," SRSConfiguration::Load() ==> DISPCFG \/home\/SRSUser\/amoreSRS\/configFileDir\/display_default.cfg\n"," SRSConfiguration::Load() ==> MAPFILE \/home\/SRSUser\/amoreSRS\/configFileDir\/GE6MappingCMScernData2015.cfg\n"," SRSConfiguration::Load() ==> PADMAPFILE \n"," SRSConfiguration::Load() ==> SAVEDMAPFILE \/home\/SRSUser\/amoreSRS\/results\/mapping.cfg\n"," SRSConfiguration::Load() ==> PEDFILE

New virtual console for a web AMORE process monitoring tool

SCRIBE nodes

SCRIBE COMPUTER NODES

/mnt/nas1/cmsgem/1C:6F:65:34:B4:8E.pcinfo	/mnt/nas1/cmsgem/40:8D:5C:1A:0A:26.pcinfo

C O M P U T E R   I N F O

Linux hohlmann_1c6f6534b48e 2.6.18-406.el5 #1 SMP Wed Jun 3 11:32:56 CEST 2015 x86_64 x86_64 x86_64 GNU/Linux
SCRIBE package installed is
Computer set for automatic AMORE analysis

Installed partitions:
major minor #blocks name

8 0 976762584 sda
8 16 976762584 sdb
8 32 244198584 sdc
8 33 244196001 sdc1
253 0 976759808 dm-0
253 1 104391 dm-1
253 2 976647577 dm-2
253 3 966393856 dm-3
253 4 10223616 dm-4
Uptime: 1663891.67 1482895.60
- - - - - - - - - - - - - - - - - - - -
M E M O R Y

total used free shared buffers cached
Mem: 5314 913 4400 0 2 115
-/+ buffers/cache: 796 4518
Swap: 9983 329 9654

> At runtime any computer node can show the status of all others nodes. New nodes are added at runtime.

FEC at Assembly sites

	v1.1	v1.2	v1.3	v6
Operational				
CERN	0	0	2	2
Delhi	0	0	0	0
FIT	3	0	2	3
Ghent	0	1	0	1
INFN-Bari	0	0	0	3
INFN-LNF	0	0	0	0
Kolkata	2	0	0	0
UNIANDES	0	0	0	1
ordered				
CERN	0	0	0	1 (0)
Delhi	0	0	1	?
FIT	1	6	0	2
Ghent	0	0	0	0
INFN-Bari	?	?	?	?
INFN-LNF	8	8	0	1
Kolkata	?	?	?	?