Pulse-height Readout for GE2/1: Synergies with HGC Front-end Chip Development

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Motivation

• Cost savings for GE2/1 project
  – A GE2/1 readout with 128 zigzag strips per sector will reduce number of channels by factor 3 relative to GE1/1 (while preserving angular resolution). Requires pulse-height measurement to calculate charge barycenter.
  – Might well obviate need for a GEB for GE2/1; could think about sending digital data from 8 hybrids directly on 8 fibers via GBT to a concentrator

• Access to more chamber performance info
  – Pulse height information
  – Long-term monitoring of gain and aging (will not be available for GE1/1)
Requirements

Need front-end electronics that

- measures **strip charges** (pulse heights) so that hit positions can be reconstructed precisely from charge sharing among zigzag strips (charge barycenter)
- can handle **polarity** of pulses as we get them on GEM readout
- integrates sufficient **number of channels** into chip (64-128 ch.)
- has sufficient **dynamic range** for strip charges
- provides **input protection** using diodes
- provides **fast timing** for pulses
- provides output for L1 trigger
  - at least a **fast OR** of all strips above threshold
  - ideally: digitized hit positions (from charge barycenter)
- is rad-hard
- **interfaces easily with CMS back end** and CMS DAQ
Chip Survey (non-exhaustive)

• APV provides charge readout, but doesn’t have fast trigger output, no on-chip digitization

• VMM chip (BNL, RD51) provides most of desired functionality, but it’s an ATLAS development…

• Idea: Look around in CMS to see what other chip developments will be done for Phase 2:

⇒ Potential candidate is FE chip being developed for High Granularity Calorimeter (HGC):

**SKIROC2-CMS chip & successors**
HGCAL Front end electronics
SKIROC2-CMS

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Disclaimer

- I’m relating information to the best of my knowledge that I have gathered from various sources of information in the HGC community
- No guarantee of 100% accuracy
SKIROC2-CMS Chip

- SKIROC chip originally developed for ILC; being adapted by FNAL for CMS; first tests by end 2015
- New chip SKIROC2-CMS (aka SKIROC2A) is a new development specifically for CMS HGC
- It is not intended to be the final HGC chip, but rather a chip that can be produced on a fast schedule (early 2016)
- Main objective is to have FE electronics in hand for first HGC beam tests in 2016
- Test results with SKIROC2-CMS will inform the design of the final FE chip for HGC
Global Chip Architecture

- ASIC is 64 channels
- 2 serial links (data L1 + trigger)
SKIROC2-CMS Characteristics

- 64 channels
- Pos. or neg. input polarity allowed
- Outputs per channel:
  1. Digitized Pulse Height
     1. small pulses up to ~ 100 fC: 10-bit ADC (Successive Approxim. Register)
     2. large saturated pulses: 12-bit TAC for Time-over-Threshold (ToT)
  2. Digitized Time-of-Arrival: 12-bit TAC (50 ps jitter)
  3. Fast discriminated output for trigger OR
- Pre-amps for each channel:
  - Fast pre-amp & shaper for trigger OR
  - Fast pre-amp for Time-of-Arrival (ToA, 5-15 ns shaping time)
  - Gain 1 & 10 “slow” preamps for pulse height (5-75 ns)
  - Shaping times of all pre-amps programmable
- 40 MHz circular analog memory, 300 ns depth
SKIROC2-CMS Analog Architecture

- Versatile preamplifier
  - Dual polarity: single first stage with input PMOS transistor (available NMOS are directly on substrate), one feedback for each polarity, high dynamic range optimization
  - Variable Rf: global 8 bits, from 10K to 2,55M
  - Variable Cf: global 6 bits, from 62fF to 4pF

- Slow shapers
  - Gain 1 and gain 10
  - Variable shaping time: global 4 bits, from 5ns to 75ns

- ToT: discriminator connected to the preamp output
- ToA made of fast shaper and fast discriminator
  - CRRC fast shaper, variable shaping time: ~ 5 to 15 ns

12 bit-ADC Ramp
Time, ssh_G1, ssh_G10 conversion
ADC test

10/8/2015
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SKIROC2-CMS Analog Architecture

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Christophe de la Taille, CMS Upgrade Week, Ischia, Sep 2015
Detector-Chip Interface

For HGC:

- Chips are wire-bonded to front-end boards (M. Miller, UCSB)
- Two front-end boards connect to a wafer with 130 Si sensors
- GBT links bring data off detector
Detector-Chip Interface

For GEM R&D:

- Could envision adapter board:
- Matches input pads on HGC front-end board to our Panasonic connector
- Plug adapter / front-end board combo into GEM
Test DAQ

Readout [P. Rubinov et al.]

- Evolutive DAQ
  - FMC cards in 6U crates (FPGA Mezzanine Card)
  - Daughterboards supporting 2 wafers
  - Ethernet readout
  - Zynq7000 based
  - Also provides power to wafers
  - Kapton flat cable and low profile connectors chosen

- Ready to manufacture

Could work with FNAL and U. Minnesota on obtaining a small DAQ test setup…
Questions to be Answered

• Sufficient diode protection?
• Can we calculate charge barycenter, i.e. strip hit position, on chip?
• Do we even need to for the trigger?
• What is the connector footprint of the HGC front-end readout board?
• …
The Upshot

• The development of the SKIROC2-CMS and the final HGC chip should be of interest to us
• They appear to provide most of what we need to get pulse height info from our chambers
• A big advantage is that this chip development will happen in CMS no matter what!
=> In some sense, it is “free” for us
• The sooner we interact with chip developers, the easier it will be to influence the design to some degree to suit our specific application
Thank you!